# A bench-test system of the visual prostheses utilizing retino-morphic spikes as the driver signals of intracortical microstimulation

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## Abstract

We developed a prototype bench-test system of the intracortical visual prostheses, in which retino-morphic point-process spike signals from our previously developed retina emulator were utilized for driving the microstimulation applied to the cerebral visual cortex. Substituting the stimulating electrodes with micro-LEDs, the system operations were verified through dry bench tests, in which the spatial pattern of stimulus outputs via 4096 channels was able to be dynamically controlled by stimulus images projected to the retina emulator.

*Keywords*: Visual prosthesis, Retino-morphic emulator, Point-process spike signal, Intracortical microstimulation

## 1. Introduction

It has been known for decades that the electrical microstimulation delivered to multiple focal sites in the primary visual cortex can be a reasonable approach for providing artificial vision to people with acquired blindness.[1,2] A recent clinical study in a blind patient reexamined and further confirmed the feasibility of the intra-cortical visual prosthesis.[3,4] Also, a recent psychophysical behavioral study in non-human primates suggested a possibility of evoking the shape perception with phosphenes by means of high-channel-count intra-cortical microstimulation.[5] For realizing a high-channel-count visual prosthesis, it is essential that the incoming information of visual scene should be processed, and delivered to the visual cortex, in a physiologically efficient and psychologically efficacious manner. It is considered that a possible solution for such a prosthesis can be learned from the biological visual system.

In the previous study, we developed a neuromorphic retinal circuit emulator[6] utilizing the Izhikevich model,[7] with which the point-process spike signals are output from 128-by-128 channels, at millisecond time resolution in response to visual events. In other previous studies, we also developed a prototype wireless system supporting the maximum of 4096 channels of intracortical microstimulation for use in animal physiological experiments.[8] In order to further advance the preclinical studies on the visual prosthesis, the present study aimed to integrate the retinal circuit emulator into the multi-channel microstimulation system, and to test the integrated operations of the system.

## 2. System Integration

As the first step of the system integration, a wired configuration was chosen for the present study. Fig. 1 outlines the wired integration. The first stage is the retinal circuit emulator (Fig. 1, uppermost), which captures the visual scene, performs the information processing, and outputs the point-process spike signals as “spike images”. Subsequently, the data packets of the spike images sent from the emulator are decompressed in a single-board computer (“Raspberry Pi” in Fig. 1), and are fed to a Field-Programmable-Gate Array (“FPGA” in Fig. 1) that provides the digital data of the stimulation parameters and the controlling signals for the microstimulator ASIC chip.[8] In the final stage, the ASIC chip generates the microstimulation current pulses through the intracortical stimulating electrodes. In this study, only one chip of the microstimulator was employed for saving the hardware resource and avoiding any complications in experiments on the system operation.

Main roles of the hardware components in the integrated system are explained in the following sections.

### *2.1 Retinal circuit emulator for image processing and spike encoding*

The details of our retinal circuit emulator have been described in the previous paper.[6] In brief, the emulator is an analog-digital hybrid hardware system consisting of a circuit board with the analog VLSI chip called silicon retina[9] (*a* in Fig. 1), an interface board with a SRAM memory chip (*b* in Fig. 1), and a FPGA board (*c* in Fig. 1). In the silicon retina, the incoming images are captured at 200 frame-per-second with the 128-by-128 array of the CMOS active-pixel sensors, and the spatial filtering found in the biological outer retina is emulated by the double-layered resistive network realized by CMOS analog circuits.[9] In the FPGA, the spatial center-surround antagonistic filtering, the linear temporal filtering, and the nonlinear gain function found in the biological inner retina are implemented by the digital signal processing.[10] Moreover, the spike firings in the retinal output neurons, namely retinal ganglion cells, are emulated by the Izhikevich model.[7] By adjusting parameter values of this model and of the above-mentioned filters and functions, the spike responses to light stimuli in the biological retinal ganglion cells (Fig.2, middle trace in Fig. 2, “mouse RGC spike”) could be reproduced in reasonable detail by the emulator (lower trace in Fig. 2, “emulator output spike”). Since the array size of the emulated retinal ganglion cells of a certain subtype is 128-by-128 in the original format,[6] the size is down-sampled to 64-by-64 channels to fit the number of the output channels of the microstimulation system[8]. The down sampling is performed in the emulator by summating the values in a 2-by-2 patch and thresholding the summated values.

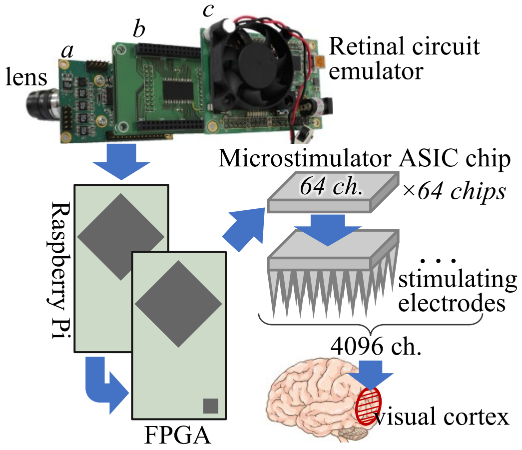

Fig.1. The hardware system configuration integrating the retinal circuit emulator [6] and the multi-channel microstimulation system.[8]

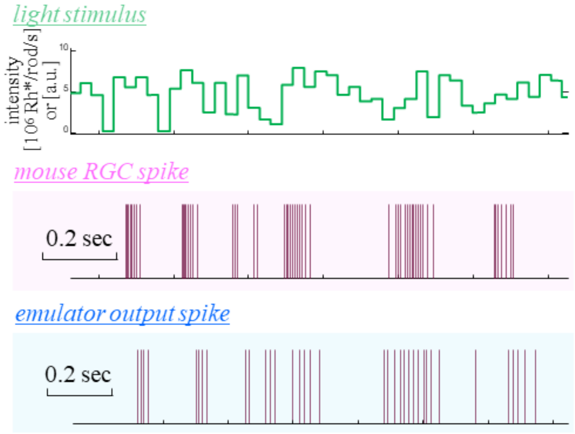

Fig.2. Example of the spike signals measured from the biological retinal ganglion cell (middle) and the output of the retinal circuit emulator (lower) in response to the light stimulus (upper)

### *2.2 Single-board computer for data managing*

The retinal circuit emulator is connected to the single-board computer (Raspberry Pi 4 Model B, Raspberry Pi Foundation, Cambridge, U.K.) by the USB2.0 standard. The data communication is made by using the Python-3.7 USB communication module, PyUSB1.1.1. In the single-board computer, each frame in a 64-by-64 array of the spike images retrieved from the emulator is first sectioned into 64 blocks, each of which is an 8-by-8 array. Subsequently, the spike binary data for each of those blocks are sent to the next stage FPGA to be used as the position data of the microstimulation channels. By sequentially sending all datasets of the 64 blocks, 64-by-64 channels of microstimulation can be achieved. The achievable frame rate in this manner was approximately 30-40 fps.

Although, in the present system, the above-mentioned data managing by the single-board computer is rather simple, it would become complicated if two sets of the retinal circuit emulator are employed for the binocular configuration and if the visual cortices in the both hemispheres are the targets of microstimulation for expanding the field of the artificial vision.

### *2.3 FPGA for microstimulator ASIC chip control*

The single-board computer is connected to the next stage FPGA (Spartan-6, Xilinx, CA, U.S.A.; XEM6010, Opal Kelly, OR, U.S.A.) with using the GPIO pins in the Raspberry Pi and the I/O pins in the FPGA board. In the FPGA, the digital codes in custom format are generated to control the microstimulator ASIC chip. Some of those determine the stimulus parameters and others are to control the circuit operations and memory registrations.[8] The spike binary data of a particular block out of the 64 blocks mentioned above were transcoded to the position data of the microstimulation channels. In addition, since an individual chip of the microstimulator is pre-assigned with an identification (ID) number of the 6-bit code, the ID code is also generated according to the location of a particular block out of the 64 blocks by the FPGA. The position data are once stored in the built-in register of the assigned microstimulator chip, and then stimulus current pulses are injected thought the output channels of the chip depending on the stored position data. The timings of the stimulus current injections are also controlled by the FPGA.

## 3. Dry Bench-Test of the Integrated Operation

### *3.1 Experimental setup*

Fig. 3 shows a photograph the experimental setup for testing the integrated operation of the system. The upper panel shows the computer disply for the stimulus image presentation and the retinal circuit emulator in front of the display. The lower pannel shows the other hardware componets of the integrated system, nemaly, the Raspberry Pi, the FPGA board, the microstimulator ASIC chip, and a micro-LED array. As shown here, a 8-by-8 micro-LED array is used intead of 64 stimulating electrodes, and thus, spatio-temporal patterns of the microstimulation are examined by imaging the spatio-temporal patterns of the LED light with using a video camera. Since only one pair of the microstimulator chip and the micro-LED array was employed, the LED light patterns were repeatedly imaged for 64 times in sequential sessions, and those images were combined off-line to form the light patterns of 4096 LEDs.

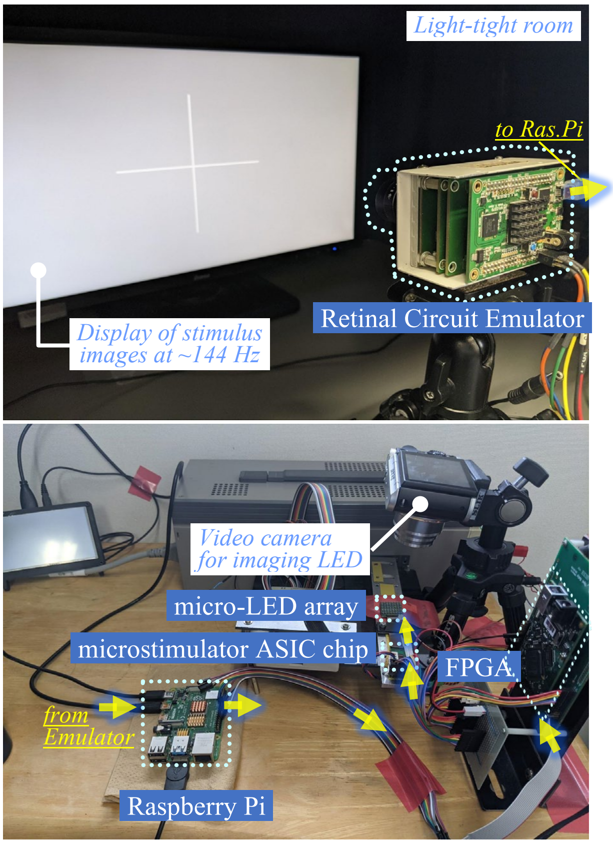

Fig.3. Experimental setup for the dry bench-test of the integrated system.

### *3.2 Experimental results*

In the experiment, the stimulus images were presented as a 10-second movie, as shown in Fig. 4*A*. This movie was repeatedly projected to the retinal circuit emulator for 64 times. As explained in the previous subsection, the LED light were imaged by the video camera, and thus, a movie file created by this video camera was sectioned into 64 movie files, each of which had a duration of 10 seconds, and then was edited off-line. Fig. 4*B*-*C* shows time lapse images of the spike image data in the 64-by-64 array sent from the retinal circuit emulator to the single-board computer (*B*) and of the output light patterns of the 4096 LEDs (*C*). Since the transient response type of the biological retinal ganglion cells was emulated by the retinal circuit emulator in this experiment, the time lapse images were taken from the time points after the onset of switching the stimulus images from one to the next. As shown in these results, the spatial patterns of the LED light (*C*) showed reasonable correspondences to those of the spike images (*B*). In some portions, the LED light patterns differed from those of the spike images. This was mainly due to mismatch among the refresh timing of the display used for the spike images, the LED blinking timing at ~39 fps (frame interval of ~25.4 msec) and the image capturing timing in the video camera, during the 64 repetitions mentioned above, and also due to the stochastic nature of the spike timings in our retinal circuit emulator.[6] Nevertheless, these results demonstrated the proper operations of the integrated system.

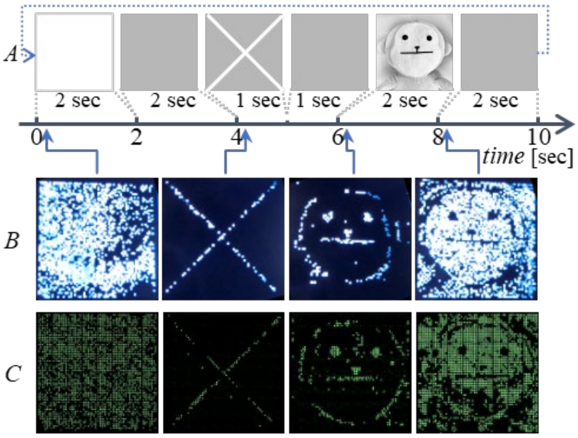

Fig. 4. Example of the experimental results. *A*) The sequence of the stimulus image presentation. *B*) The 64-by-64 spike images in response to the stimulus images shown in *A*. *C*) The final output patterns of the 64-by-64 LED light driven by the spike images shown in *B*.

## 4. Discussions

In the present study, we integrated the retinal circuit emulator into the multi-channel microstimulation system and verified the system operation through the dry bench-test. If the data communication rate between the retinal circuit emulator and the single-board computer is made faster, and/or if the data managing performed in the single-board computer is implanted in the FPGA, then the frame rate of the stimulus outputs is expected to be shortened. From the physiological point of view, 50 to 100 fps would be sufficient for exciting the neural circuits in the visual cortex with the microstimulation.[11,12]

## Acknowledgements

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