Research On Embedded Electrical Impedance Measurement System

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Abstract

This paper develops an impedance measurement system based on S3C6410 processor. An OK6410 host board as the controller platform and an AD5933 chip is used to collect impedance data, and the data is exchanged with the controller with IIC bus protocol. Comparing with the measuring result of the Wayne Kerr 6800B impedance analyzer with the accuracy of 0.05%. The system has the behaviors as lower relative error 0.422% and higher signal-to-noise (SNR) ratio 64.11dB. After calculation, the average absolute error of the impedance phase of the system is 0.527°. The tests results verified that the system is reliable and flexible with a wide application prospect.

Keywords: impedance measurement, embedded system, AD5933, S3C6410

1. Introduction

1.1. *Impedance measurement technology*

Impedance measurement technology is an important part of electronic measurement technology.

In the field of industrial production, the oil moisture content can be measured by measuring the impedance of multi-phase flow [1-2]. In the field of biomedicine, the pulmonary respiratory process can be visualized and monitored by measuring the impedance information of human lungs [3-4].

It is widely used in biomedical, electrochemical, industrial control, power grid control, etc.

1.2. *Principle of impedance measurement*

Impedance plays a very important role in the related research on the electrical properties of materials. From the impedance, a large number of electrical parameters can be deduced to comprehensively analyze the substances. In physical electronics, impedance indicating the degree of obstruction of an object by current, and is the ratio of voltage U to current I, expressed in ohms (Ω), represented by the letter Z. In general, the impedance is a complex, the real part representing the resistance features, labeled by R; the imaginary part represents feature, labeled by X. Z can be expressed as follow:

$$Z = \frac{U}{I} = R + jX = |Z|\angle\theta \qquad (1)$$

Where, is the amplitude of impedance, is the phase angle, and the formulas for calculating and are according to Eqs. (2) and (3).

$$|Z| = \sqrt{R^2 + X^2} \qquad (2)$$

$$\theta = \arctan\frac{X}{R} \qquad (3)$$

The conversion formulas of the real part and the imaginary part are using Eqs. (4) and (5).

$$R = |Z| \cos\theta \quad (4)$$

$$X = |Z| \sin\theta \quad (5)$$

1.3. *Measuring system frame*

In the research, an OK6410 board with embedded processor S3C6410 is responsible for running the operating system and measuring programs. The data acquisition and signal conditioning are carried out by AD5933 chip. When it working, the instructions are sent to the AD5933 chip through the analog IIC bus, which make the measurement circuit [5-6] simple. The AD5933 transmits a measured signal to the host board. After a series of conversions and measurements, the signal is returned to the host board and a measurement is finished.

2.2. *DC-blocking drive circuit*

When measuring an object which unknown impedance, the AD5933 will output a sinusoidal excitation signal with a significant DC component, which will cause polarization and affect the measuring precision in TABLE 1. It shows the output impedances at different gains and frequencies at 5V and 2.7V. In addition, the internal amplifier of the AD5933 has a high output impedance, which can affect the output signal adversely. The DC bias and output impedance of different output voltages under the voltage supply of 3.3V are shown in Table 1.

The output voltage of this system is 1.98V. The DC offset is fixed to 1.48V, and the DC bias voltage of the receiving end of AD5933 is 1.65V. There is a potential difference of 0.17V, which is easy to cause polarization occurs at the output and receiver.

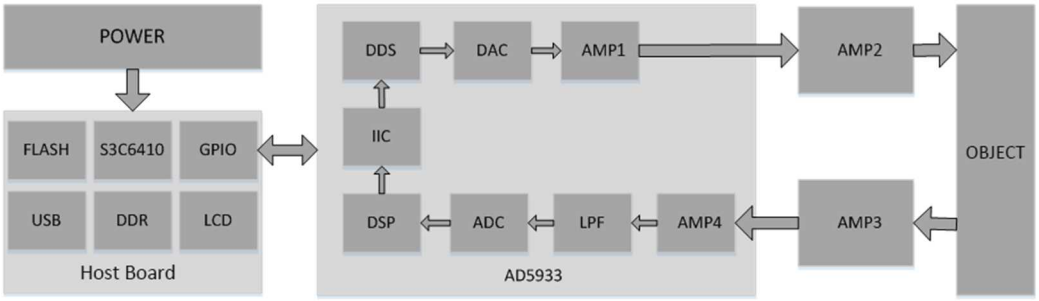


Fig. 1. Hardware system frame.

Finally, the controller output the processing results to the operating platform. The system frame is shown as Fig. 1.

2. Hardware design

2.1. *Data collection*

We use a direct digital frequency synthesizer (DDS) to generate an alternative exciting current with short conversion time, high frequency resolution and flexible output. The signal is sampled using a high-speed analog to digital converter (ADC). Then, the digital signal processor (DSP) inside the AD5933 demodulate the signals BY Fourier transform, the real and imaginary information of the signals are extracted from the measured impedance [7-8].

Table 1. DC bias and output impedance of each excitation voltage.

Output excitation voltage	DC bias voltage	Output impedance typical
1.98V	1.48V	200Ω
0.97V	0.76V	2.4kΩ
383mv	0.31V	1.0kΩ
198mv	0.173V	600Ω

To eliminate the 1.48V DC bias, a 47nF capacitor and two 50kΩ resistors are used to obtain a DC bias VDD/2 = 1.65V, equivalent resistance R = 25KΩ. The circuit is shown in the Fig. 2. The cut-off frequency is set to 135 Hz, which is much lower than the lowest system measuring frequency 10 kHz. The interference to the excitation signal can be ignored. Resetting the DC offset reduces the polarization and improves the accuracy of the device.

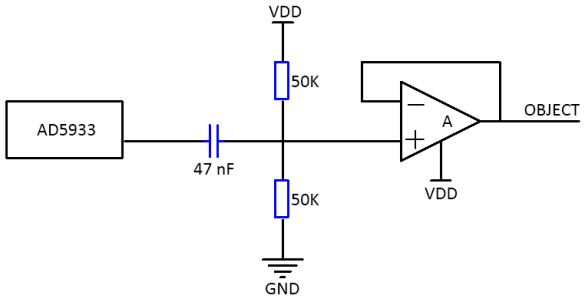


Fig. 2. Signal excitation circuit.

2.3. *Receiving circuit*

The current-voltage amplifier of the AD5933 is susceptible to the bias current, offset voltage, and CMRR of itself, which resulting in inaccurate measurements. By setting an amplifier with excellent characteristics such as low offset voltage and low bias current at the receiving port of the AD5933, the adverse effects of the self-integrated amplifier can be eliminated and the measurement accuracy can be improved. In this design, an AD8606 chip is adopted to build the excitation circuit. The AD8606 has dual channels that can be designed as a voltage follower and the required external converter simultaneously on a single chip, which can reduce the circuit complexity, save the manufacturing costs, and avoid the dual channels unbalance. It also can avoid inconsistencies caused by the using different amplifiers. The circuit is shown in Fig.3.

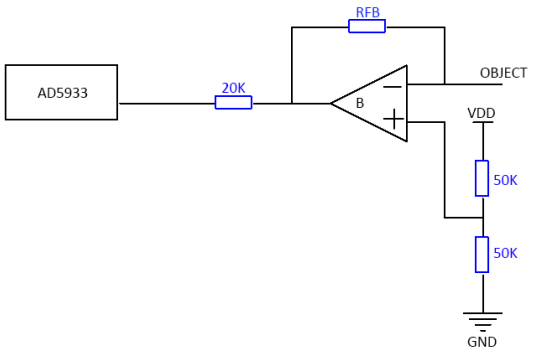


Fig. 3. AD5933 receiver circuit.

2.4. *Feedback resistor*

The measured signal is transferred to the ADC for analog-to-digital conversion. In this step, the input voltage of the ADC needs to be adjusted by some setting parameters such as feedback resistor and gains to ensure it within the linear input range of the ADC. If the input voltage is too large, the ADC can be saturated and errors occurs. If the input voltage is too small, it cannot carry enough measuring information and is susceptible to noise and reduces measurement accuracy.

Due to the requirements of the measurement parameters and the several factors affecting the output voltage, the excitation voltage and the PGA gain can be fixed to a setting point. The feedback resistor needs to be properly selected according to the magnitude of the unknown impedance to ensure the input voltage within the range of the ADC. The feedback resistor needs to select a precision resistor with high precision, capacitive and inductive impedance.

A series of feedback resistor is considered to support 100Ω-200kΩ measurement listed in Table 2, and the overall design of the data acquisition circuit is shown as Fig. 4.

Table 2. Feedback resistance and its impedance measurement range.

Measurement Range	Feedback Resistor
100Ω-1kΩ	100Ω
1kΩ-10kΩ	1kΩ
2kΩ-20kΩ	2kΩ
10kΩ-100kΩ	10kΩ
20KΩ-200kΩ	20kΩ

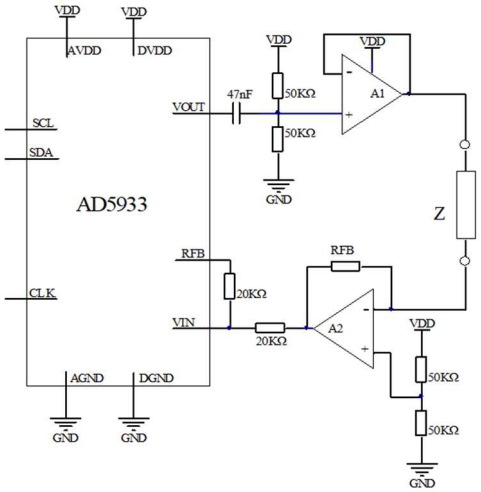


Fig. 4. Data acquisition circuit. Including AD5933 chip and signal conditioning circuit, DC amplifier circuit, receiver circuit and feedback resistor

In measuring, one of the feedback resistor is selected to guarantee most approximate to the measured object. The hardware module is shown as Fig. 5.

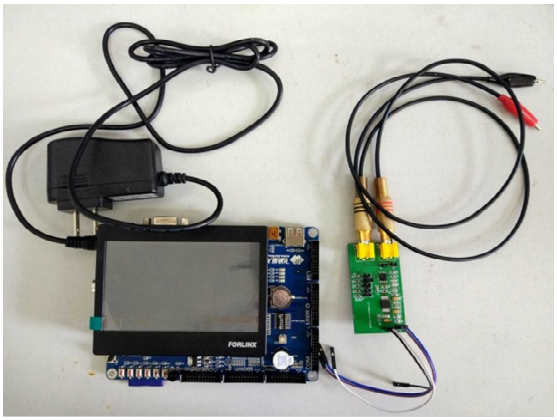


Fig. 5. Hardware module. Including operation platform, data acquisition module, and fixture.

3. System test

3.1. *Accuracy and SNR*

Taking 2kΩ testing as an example, we select 4.7kΩ as the feedback resistor, the excitation voltage is 1.98 V, and the PGA gain is 1. The test begins at 10 kHz with 1kHzincremental increase until 100 kHz. There are 91 testing values acquired. The testing is repeated 100 times. The relative error and SNR ratio at each frequency are calculated according to Eq. (6) and (7).

$$E_i = \frac{\bar{X}_i - X_t}{X_t} \times 100\% \quad (6)$$

$$SNR_i = -20lg\left(\sqrt{\frac{1}{n-1}\sum_i^n (X_i - \bar{X}_i)^2}\,/\bar{X}_i\right) \quad (7)$$

$\bar{X}_i$ is the average value of the measured impedance at the ith frequency, X_t is the actual value measured by the Wayne Kerr 6500B impedance analyzer, $\bar{X}_i$ is the measured impedance at the ith frequency, E is the relative error, and SNR is the signal noise ratio, n is the number of measurements.

The Wayne Kerr 6500B impedance analyzer measures the actual impedance of the resistor with an accuracy of 0.05%. Then the average relative error and signal to noise ratio of the feedback path are calculated. The other four feedback paths are tested in the same way as above. The performance specifications of the five feedback paths are shown in Table 3.

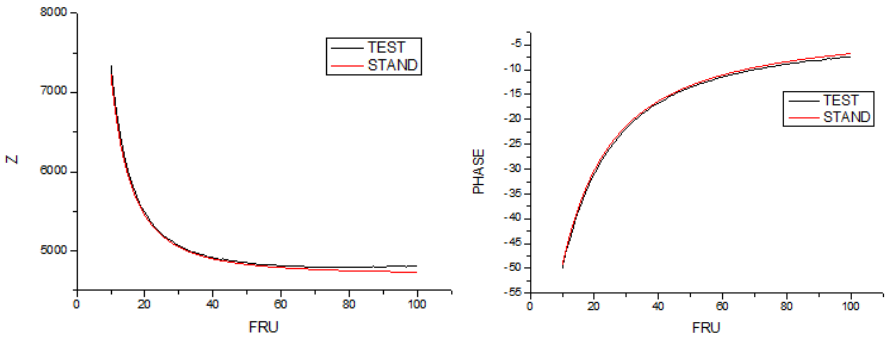
Table 3. Relative error and snr ratio of each of the five feedback paths.

Tested resistance	Feedback resistance	Relative error (%)	SNR(dB)
100	330	0.56	68.14
1k	4.7k	0.50	65.63
2k	4.7k	0.52	70.55
10k	51k	0.34	54.59
20k	51k	0.19	61.66

The average error of the system as 0.422%, and the SNR ratio is 64.11dB. The results show that the system has higher accuracy and signal to noise ratio.

3.2. *Phase Accuracy Test*

The system excitation voltage to 1.98 V. The test begins at 10 kHz with 1 kHz incremental till 100 kHz and there are 91 testing values acquired. The testing is repeated 100 times. After taking the average of the measured values, the absolute error of each frequency point is calculated. The Wayne Kerr 6800B impedance analyzer with an accuracy of 0.05% measures the phase data used for calibration. The calculated phase absolute error is shown in Table 4, where P indicates parallel and S indicates series.



(a) (b)

Fig. 6. Comparing the measurement results of this system with the measurement results of the impedance analyzer, the black line is the result of the system, and the red line is the Wayne Kerr 6800B impedance analyzer result. Flow (a) is impedance data, and (b) is phase data.

Table 4 Absolute phase error of each r-c circuit.

R(Ω)	C(nF)	Connect type	Absolute error (°)
330	28	Parallel	1.664
330	32	Series	0.266
4.7k	3	Parallel	1.048
4.7k	3	Series	0.229
4.7k	16	Parallel	0.441
4.7k	16	Series	0.222
20k	3	Parallel	0.754
20k	3	Series	0.132
20k	16	Parallel	0.382
20k	16	Series	0.132

Finally, calculate the average phase absolute error of the system. The applied experiments on 4.7kΩ and 3nf series R-C circuits, and use origin 8.5 to compare the two data, is shown in Fig. 6.

After calculation, the average absolute error of the impedance phase of the system is 0.527°, which indicates that the system has good measurement performance for phase.

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