

Compensating Temperature-Dependent Characteristics of a Subthreshold-MOSFET Analog Silicon Neuron

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Abstract

Analog silicon neurons are neuro-mimetic VLSI (very-large-scale-integrated) circuits that replicate the electrophysiological behavior of animal nerve tissue. This research focuses on the temperature sensitivity of a subthreshold-MOSFET analog silicon neuron. Subthreshold operation of CMOS transistors allows for low power consumption, but is also drastically sensitive to temperature changes. This critical issue must be addressed before these circuits can be implemented into massive networks to develop future neuromorphic technologies.

Keywords: neuromorphic engineering, analog VLSI, silicon neurons

1. Introduction

The field of neuromorphic engineering seeks to design circuits that mimic the electrophysiological behavior and network structure of neurons to create biologically-inspired or neuromimetic technology that can perform calculations in ways fundamentally different from traditional digital computers. Motivations for research in this field include developing brain-like computers and bio-silico hybrid systems for medical devices.

Analog silicon neurons are electronic circuits that exploit the characteristics of transistors to mimic how nerve cells control membrane potential. These circuits operate in continuous time, can replicate a variety of spike shapes and spiking behavior, and require low power^{1,2,3,4}. They are expected to be a promising tool to construct neuromorphic systems. However, many technical challenges must be addressed before these circuits can be implemented in large-scale networks. A possible method to solve a key issue, temperature sensitivity, is to actively tune the circuit parameters depending on temperature. We report our approach in which appropriate parameter sets for several

temperatures are found and parameter sets for intermediary temperatures are obtained by interpolation.

2. Circuit Description

The circuit used in this research (Fig. 1) is an ultra-low power VLSI silicon neuron based on qualitative neuronal modeling¹, which seeks to use judicious approximation and mathematical understanding⁵ to convert the model of membrane potential to equations with fewer variables that are more suitable for circuit implementation. In the model for this circuit, variable v represents membrane potential and variable n represents abstracted ionic activity. The value of each variable is calculated by subtracting the voltage over each capacitor from V_{dd} (1.0V). These two variables control the output currents of transconductance circuit components $f_x(v)$, $g_x(v)$ ($x=v, n$), and $r(n)$ that charge and discharge capacitors attached to the v -block and n -block within the circuit. This circuit was shown to support the dynamical behaviors of Class I and II neurons in the Hodgkin's classification⁶. The system equations of this model are as follows:

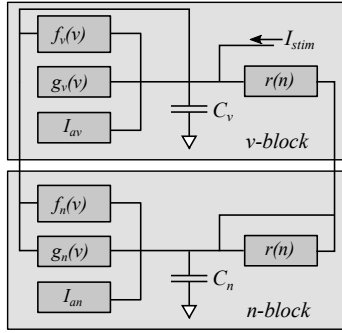


Fig. 1. Circuit block diagram of the silicon neuron circuit.

$$C_v \frac{dv}{dt} = f_v(v) - g_v(v) + I_{av} - r(n) + I_{stim} \quad (1)$$

$$C_n \frac{dv}{dt} = f_n(v) - g_n(v) + I_{an} - r(n) \quad (2)$$

I_{stim} is an external stimulus current, and I_{av} and I_{an} are constant currents. The current-voltage characteristics of the $f_x(v)$, $g_x(v)$ ($x=v,n$), and $r(n)$ components are expressed by the following sigmoidal relationships:

$$f_x(v) = M_x / (1 + \exp(-\frac{\kappa}{U_T}(v - \delta_x))) \quad (3)$$

$$g_x(v) = I_0 \sqrt{\exp(\frac{\kappa}{U_T} \theta_x) / (1 + \exp(-\frac{\kappa}{U_T}(v - \theta_x)))} \quad (4)$$

$$r(n) = I_0 \sqrt{\exp(\frac{\kappa}{U_T} \theta_r) / (1 + \exp(-\frac{\kappa}{U_T}(v - \theta_r)))} \quad (5)$$

I_0 is the PMOS transistor off-current, U_T is the thermal voltage (~ 26 mV at room temperature), and κ is the capacitive coupling ratio. Parameters M_x , θ_x , δ_x ($x=v,n$), and θ_r can be tuned by bias voltages applied to the circuit. All transistors are operated in the subthreshold regime. Figure 2 (a) shows a differential pair attached to a current mirror used for $f_v(v)$ and $f_n(v)$. Figure 2 (b) shows the circuit used for $g_v(v)$, $g_n(v)$, and $r(n)$. This circuit is a cascoded transistor with source degeneration and a detached bulk voltage.

This silicon neuron circuit includes a nullcline-drawing function which assists in the diagramming of a phase plane to evaluate the circuit's dynamical structure. For example, a sigmoidally shaped n -nullcline and cubic-shaped v -nullcline that cross at 3 distinct points yields Class I behavior in the Hodgkin's classification

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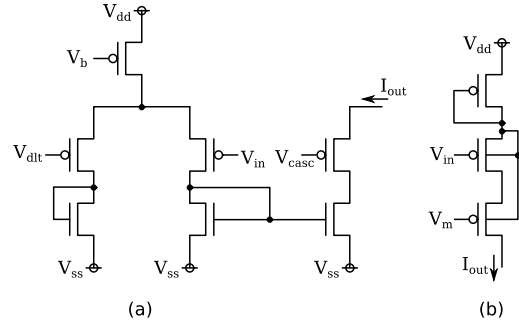
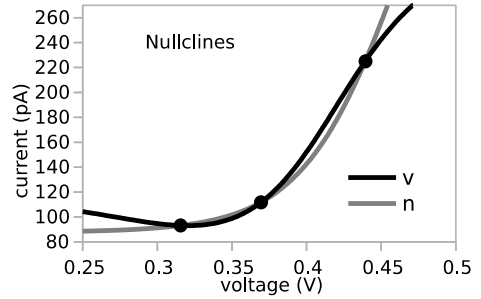

 Fig. 2. Circuit components. (a) $f_v(v)$ and $f_n(v)$, (b) $g_v(v)$, $g_n(v)$, and $r(n)$.


Fig. 3. Nullclines in Class I mode.

(Fig. 3). The points are characterized mathematically through analysis with nonlinear dynamics⁵.

The temperature sensitivity of this circuit originates in the intrinsic temperature sensitivity of MOSFETs in the subthreshold regime. Figure 4 illustrates periodic spiking behavior in the Class I mode in response to a 4 pA sustained stimulus over a narrow range of temperatures from 25 to 26.5°C. The stimulus begins at 0.2 seconds. As can be seen from the figure, the spiking frequency varies by temperature, and ceases at 26.5°C.

3. Parameter Compensation by Interpolation

In this work, we suppose a temperature sensitivity management algorithm in which the parameter voltages applied to the circuit are adjusted depending on the temperature. Such an algorithm will be used by simple on-chip components to control circuit parameters, thus complementing the low-power characteristics of the circuit. We examined an approach to finding appropriate parameter sets for each temperature which maintain the important characteristics of a neuron: spike frequency in

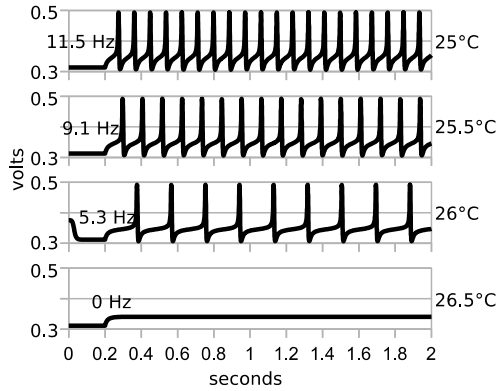


Fig. 4. Periodic spiking at different temperatures.

response to sustained stimuli and the threshold pulse stimulus for spike generation.

First, circuit behavior was analyzed at 27°C and these results were considered the benchmark for operation at other temperatures. The data recorded included frequency response to 5 pA and 10 pA sustained stimuli, and the threshold current I_{th} of a pulse stimulus (500μs pulse width) required to generate an action potential. The v and n -nullclines were also plotted. Next, the circuit was simulated at 17, 22, 32, and 37°C. Selected circuit parameters were tuned to generate behavior that most closely matched the 27°C benchmark. The nullcline-drawing function was used extensively, with the conjecture that similarly shaped nullclines lead to similar circuit behavior. Finally, the tuned parameter sets were input into a script which interpolates functions from these data points and returns circuit parameter sets for any intermediary temperature. This procedure was performed with the Class I setting simulated by the Spectre circuit simulator.

4. Simulation Results

4.1. Simple approach

We selected 5 significant circuit parameters because exploring high-dimensional parameter space is inefficient. The tail current of the $f_n(v)$ component, the bias voltages of the $g_v(v)$ and $r(n)$ components, and the constant current sources I_{av} and I_{an} were tuned with all other circuit parameters held constant. The $g_n(v)$ component was turned off. Table 1 shows the best parameter sets which most closely replicated the

benchmark behavior at each temperature. The bottom 3 rows of the table show the circuit behavior at each temperature. The script was then used to generate parameter sets for all intermediary temperatures in 0.5°C steps from 17 to 37°C. Parameters were rounded to the nearest 0.5 mV. These 42 parameter sets were then simulated with Spectre in their corresponding temperatures. The "simple" column in Table 2 summarizes the results. "Average % change" refers to the average percent difference from the benchmark behavior. Firing frequencies were relatively close to the benchmark behavior, with the exception of the 5 pA stimulus at 29°C which failed to fire. The threshold current showed a downward trend with higher values above 200 pA at lower temperatures and lower values around 140 pA at higher temperatures.

Table 1. Parameter sets with corresponding circuit behavior using the simple approach

Temperature (°C)	17	22	27	32	37
gv_Vm (mV)	388	417	432	443	449.5
fn_Vb (mV)	257	248	237	231	219
Iav_Vin (mV)	434	450	461	468.5	473.5
Ian_Vin (mV)	420	449.5	464.5	475	481.5
rn_Vm (mV)	480.5	462.5	445	430	415
I_{th} (pA)	201	185	178.5	164	147
5 pA response (Hz)	16.3	15.8	15.1	15.7	18.5
10 pA response (Hz)	39	38.8	36.2	38.7	39.4

Table 2. Analysis of interpolation results

	simple	full
5 pA stim average freq. (Hz)	15.8	11.9
5 pA stim average % change	5.2	-9.3
5 pA stim frequency range (Hz)	3.7–27.1	2.4–26.1
10 pA stim average freq. (Hz)	38.7	35.5
10 pA stim average % change	6.8	-0.6
10 pA stim freq. range (Hz)	34.6–43.2	26.8–40.4
Average threshold current I_{th} (pA)	172	185.4
Average I_{th} % change	-3.6	-0.1
I_{th} range (pA)	115.5–216	131–303.5

Table 3. Parameter sets with corresponding circuit behavior using the full-parameter approach

Temperature (°C)	17	22	27	32	37
fv_Vb (mV)	256.5	248.5	238	230	219
fv_Vdlt (mV)	567	571	580	588	596
gv_Vm (mV)	464	451	432	420	398
fn_Vb (mV)	255	246	237	228.5	219
fn_Vdlt (mV)	517	520	520	521	524
Iav_Vin (mV)	437	452	461	469	472
gn_Vm (mV)	220	178.5	156	132.5	113
Ian_Vin (mV)	395	445.5	461	473	479
rn_Vm (mV)	480.5	463.5	445	427	413
I_{th} (pA)	250	191	186	169	145
5 pA response (Hz)	13.3	17.1	13.2	13.2	13.2
10 pA response (Hz)	32.7	36.5	35.7	36.0	38.6

4.2. Full-parameter approach

A second approach augments the strategy used above by incorporating all the influential circuit parameters including the tail current and offset voltage of $f_v(v)$, the offset voltage of $f_n(v)$, and the bias voltage of $g_n(v)$. First, each of the circuit components were simulated individually and circuit parameters were sought that maintained I - V characteristics over a range of temperatures. These parameters were then used as a starting point for tuning the entire circuit at different temperatures. Focus was placed on matching the nullclines as closely as possible. Through analysis of the individual components, it was discovered that the $g_v(v)$, and $g_n(v)$ components experience a temperature induced offset, which can be compensated for by tuning the offset voltages of the $f_v(v)$ and $f_n(v)$ components.

The parameters for the pillar temperatures are listed in Table 3. Those for the intermediary temperatures in the range 17–37°C in 0.5°C steps were determined in the same way as in the previous approach. The "full" column in Table 2 shows the results of the Spectre simulations. I_{th} showed a downward trend and the firing frequencies were relatively close to the benchmark, but the 5 pA sustained stimulus failed to induce periodic spiking at 17.5–21°, 29.5°, 34.5°, 35.5°, and 36.5°C. While the temperature compensation with this approach was less effective, nullclines that more accurately matched the benchmark were obtained, suggesting that future modifications may yield better results.

5. Discussion

The above results can be improved by setting the interpolation script to return parameters rounded to the nearest 0.1 mV, but this accuracy would be difficult to replicate with real-world circuits because of thermal noise and other restrictions including the limited precision of bias voltage generator circuits.

The relative success of the simple approach suggests that limiting the available parameters leads to a smoother progression of values over a range of temperatures, allowing more success in intermediary steps. The full-parameter approach in contrast offered too much fine tuning capability. At a given temperature, some parameters were tuned more aggressively than others, depending on which yielded the most desirable behavior. This is a potential cause of the problems in the intermediary steps. Using a meta-heuristic algorithm to obtain the pillar parameter sets may solve this problem.

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