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Digital-signal improvement-method using Pareto optimization

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Abstract Recently, propagating digital signals with low distortion in PCB (printed circuit board) traces is getting difficult more and more as the frequency increases. In order to solve this problem, we have proposed "Segmental Transmission Line (STL)". In the STL, a transmission line is divided into multiple segments of individual characteristic impedance. The multiple segments are designed to improve the waveform distortion on the transmission line by solving a combinatorial explosion using genetic algorithm. In this paper, we try to improve signal integrity at two points using the STL. In order to achieve the signal integrity improvement at two points, we use the multi-objective GA and pareto-optimal-solutions. We conducted experiments with simulation and an STL prototype using real PCBs. As a result, at two observation points on simulation, logical margins in the STL were improved 3.3 times and 3.0 times simultaneously in their maximum, respectively. And at two observation points in the STL prototype, logical margins were improved 1.7 times and 2.0 times simultaneously, respectively. The result thus indicates that the STL has high ability to improve digital-signal waveform at multiple points simultaneously.

Keywords Signal Integrity, STL, Transmission Line, Genetic Algorithms, Pareto-optimal-solutions

I. Introduction

Signals of GHz frequency, the wavelengths of which are less than 15cm and are shorter than sizes PCBs, are terribly distorted at the impedance mismatching points in the PCB traces.

They have used conventional impedance-matching techniques [1][2] to improve the distorted waveforms usually. These techniques works well up to hundreds MHz, but will not work well at more than GHz.

In order to solve this problem and to ensure the signal integrity we have proposed a novel transmission line called "Segmental Transmission Line (STL)" [3] .

In the STL, a transmission line is divided into multiple segments of individual characteristic impedance. In this structure, noises are generated purposely at the segments boundaries to cancel the target noises, which occur due to the impedance mismatching between the transmission line and the devices connected to the transmission line.

In our previous paper, we have already shown effectiveness to GHz-frequency signal at single point using computer simulation and on STL prototype fabricated in real PCBs[4][5]. These STL boards were designed in the MHz-frequency targeting to the GHz-frequency by lengthening the wire (trace) length in proportion to the ration between the MHz and GHz frequencies.

In this paper, we try to improve signal integrity at multiple points using STL and to show its effectiveness using an STL prototype as well as computer simulaition.

II. Segmental Transmission Line

The idea of STL is completely different from the conventional methods such as [1],[2], which aim to decrease noise-emissions.

In the STL, we use counter approach to the conventional ones. Figure 1 shows an overview of STL and its segment-model. And Fig. 2 shows a model of the STL. In the STL, we use noises that are generated purposely at impedance mismatching points to cancel the target noises. To generate these noises purposely, a transmission line is divided into multiple segments which have different impedances and lengths, respectively. Impedance of a segment is function of a segment-width.

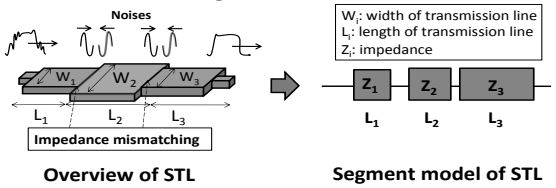

Fig. 1 Outline of STL

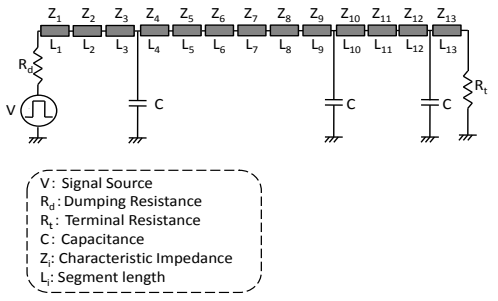

Fig. 2 STL Model

III. STL design methodology using Genetic Algorithms

In the STL, it is necessary to obtain the best, or semi-best impedance and length combination. In the case of complete search of combination, for example, 10 widths and 100 lengths for each of 10 segments results in the combination of $(10 * 100)^{10} = 1.0 * 10^{30}$. It is clearly impossible to calculate all of them, and this difficulty is called combinatorial explosion. In order to overcome this difficulty, we use Genetic Algorithms (GA) [6] to the STL design.

In the GA for the STL design, two kinds of genes are used. One is for the segment-width and the other is for the segment-length. Figure 3 shows the STL design system named STL-Designer, which is composed of a newly developed GA calculation-loop specialized for the STL and the circuit simulator SPICE. Figure 4 shows the gene and chromosome configuration of GA applied to the STL. As shown in the figure, a characteristic impedance and its corresponding length forms a pair of genes in a chromosome.

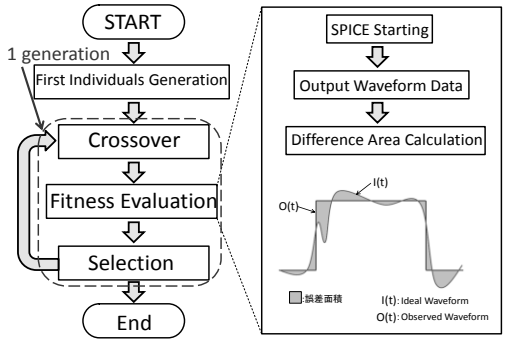

Fig. 3 STL-Designer

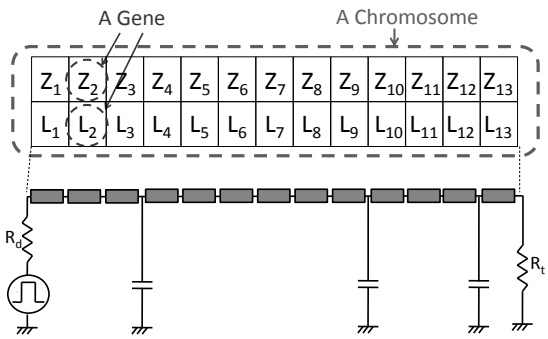

Fig. 4 Gene and Chromosome Constitution

IV. Multi-objective GA and Pareto solutions

To achieve the signal integrity improvement at multiple points, the waveforms at the observation points must be optimized simultaneously. We thus use the multi-objective GA and pareto-optimal-solution [8] to meet the design requirement. Figure 4 shows a chart of the pareto-optimal-solution. Pareto-optimal-solutions is a set of the solutions which cannot be put above the others.

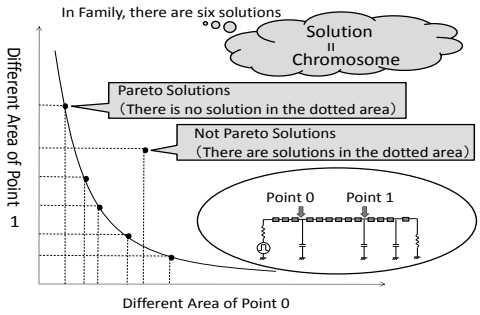

Fig. 5 Pareto optimization solution

V. Signal-Integrity improvement at multiple points on the computer simulation

In the STL design, or in the simulation, we used the circuit simulator ngspice [7] as the SPICE shown in Fig. 3. Figure 6 shows the circuit-diagram of the scale-up STL prototype for 150MHz clock-signal targeted to 1GHz. This model assumes the bus line connecting a CPU with 3 memory modules. The transmission line of 1-m long is divided into 12 segments. Three capacitors of 24pF each represent three device-inputs, e.g., memory modules connected to the transmission line. Point 0 and Point 1 in Fig. 6 are the target or observation points in the STL design. And the solution obtained in the STL is shown in Fig. 7.

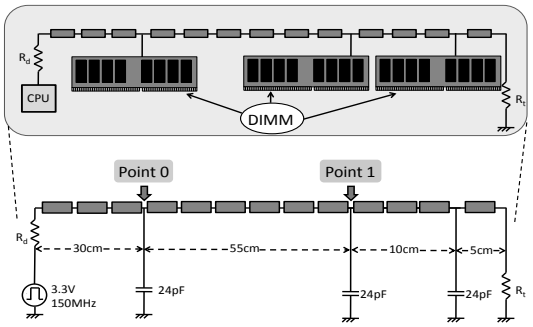

Fig. 6 Circuit-diagram of STL applied to bus system

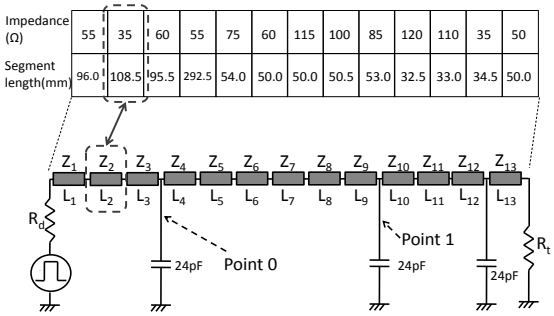

Fig. 7 Solution of GA applied to STL

In Fig. 8, distorted waveforms of red waves in the left column were observed in the conventional transmission line of homogeneous characteristic impedance of 50 ohm at Point 0 and Point1, respectively. The distorted waveforms were well improved in the STL as shown in the red waves in the right column. Blue

waveforms in the figure, which are all the same, are the waveforms observed at Point 0 and Point 1 if no capacitors are connected in the transmission line. The blue waveform was thus used as the target or teacher waveform in the design.

The results shown in Fig. 8 are summarized in Tab. 1. Improvement ratios are also shown in the parenthesis. High improvement ratios are obtained except the fall-delay time in Point 1.

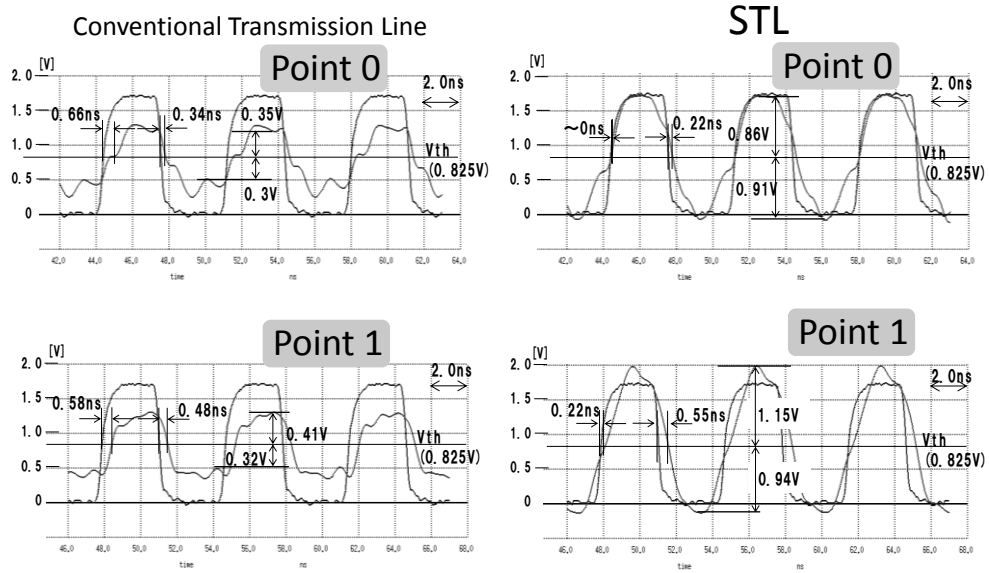

Fig. 8 Comparison of waveforms designed at Point 0

Table. 1 Summary of simulation results

() : Logical Margin Improvement Ratio and Delay Time Shortening Percentage

		High Logical Margin [V]	Low Logical Margin [V]	Delay Time (Rise) [ns]	Delay Time (Fall) [ns]
Point 0	Conventional Transmission Line	0.35	0.3	0.66	0.34
	STL	0.86 (2.5)	0.91 (3.0)	< 0.1ns (< 0.15)	0.22 (0.65)
Point 1	Conventional Transmission Line	0.41	0.32	0.58	0.48
	STL	1.15 (3.3)	0.94 (3.1)	0.22 (0.38)	0.55 (1.1)

VI. Signal Integrity improvement at multiple points in the STL prototype

Figure 9 shows photographs of the prototypes of conventional transmission line and of STL. Figure 10 shows the measurement-environment schematically. Signals from the pulse generator are put into the FPGA, which is used to reshape the waveform, and the outputs from the FPGA are input to the prototype board. The waveforms are observed by the digital storage oscilloscope of 2GHz bandwidth through an active prove.

The waveforms observed by the oscilloscope are shown in Fig. 11, which are corresponding to Fig. 8 (no teacher waveforms in Fig. 8 are shown in Fig. 11). Delay times are not measured in Fig. 11 due to some restriction in the measurement environment.

Declines in amplitudes in the conventional transmission line, which come from the waveform distortions, are well improved in the STL. The improvement ratios however are not so high as in the design, or simulation in Fig. 8. The results shown in Fig. 11 are also summarized in Tab. 2 as Tab.1.

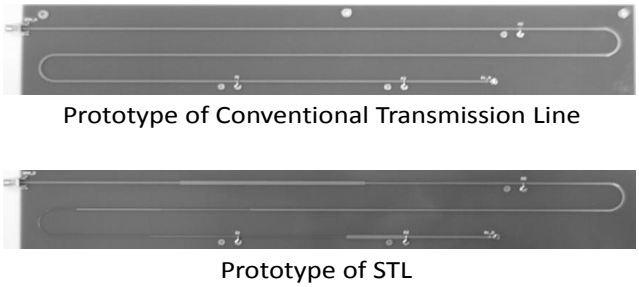

Fig. 9 Photographs of prototypes

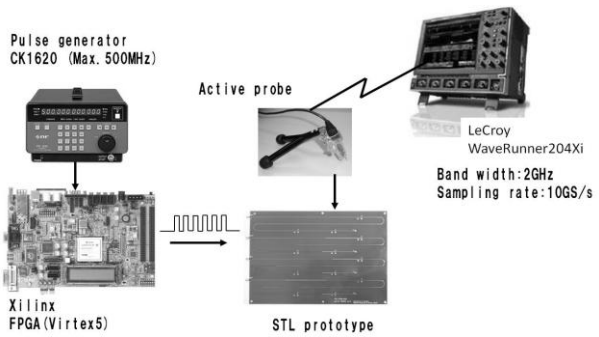

Fig. 10 Measurement environment

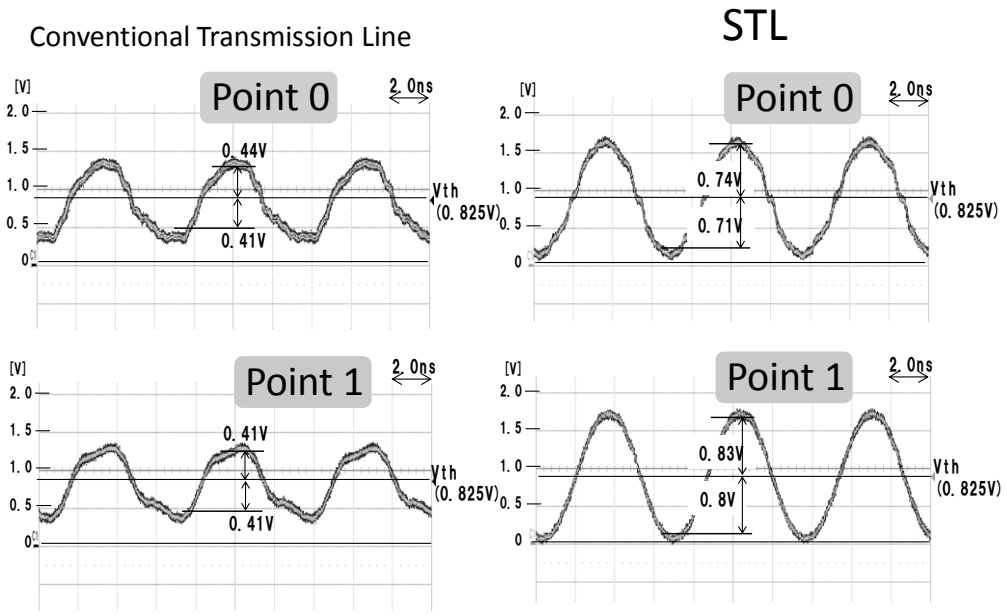

Fig. 11 Comparison of Waveforms measured at Point0 in prototypes)

Table. 2 Summary of measurement results

() : Logical Margin Improvement Ratio and Delay Time Shortening Percentage

		High Logical Margin[V]	Low Logical Margin[V]
Point 0	Conventional Transmission Line	0.44	0.41
	STL	0.74 (1.7)	0.71 (1.7)
Point 1	Conventional Transmission Line	0.41	0.41
	STL	0.83 (2.0)	0.80 (2.0)

VII. Conclusions and further works

In the simulation experiments, STL showed the maximum improvement ratios of 3.0 and 3.3 at Point 0 and Point 1, respectively in terms of the logical margin. And it also decreased the rise-time delay to less than 15% at Point 0 and the fall-time delay to 38% at Point 1 at Point 1, while the fall-time delay at Point 1 increased 10%.

In the prototype experiments, the STL showed the maximum improvement ratios of 1.7 and 2,0 at Point 0 and Point 1, respectively in terms of the logical margin.

The results clearly indicate that the STL has high ability to improve digital-signal waveform improvement at multiple points simultaneously.

Followings are further works: the fall-delay-time at Point 1 needs to be improved and accuracy of the signal integrity at two points needs to be improved and increased.

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