Digital-signal-waveform improvement on VLSI packaging including inductances

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Abstract: As digital-signal frequency in PCBs (Printed Circuit Boards) increases, waveform-distortion, or the Signal Integrity (SI) problem is getting serious more and more. The reason why the SI becomes serious is that wires, or traces need to be regard as transmission lines, which are sensitive to electric noises. In order to overcome this problem, we have already proposed a novel methodology called STL (Segmental Transmission Line), and have also shown its effectiveness using computer-simulation and fundamental prototypes. In the STL design however, combinatorial explosion problem occurs as a big problem. To solve this problem, Genetic Algorithms (GA) is used to design STL. In this paper, we newly apply the STL to the bus system that includes inductances, which come from the VLSI packaging. We evaluated the STL on the simulation experiments and the actual experiments using prototypes, and obtained the maximum improvement ratio of 1.53 in the actual experiment.

Keywords: Signal Integrity, Transmission Line, Genetic Algorithms, Inductance, Printed Circuit Board

I. INTRODUCTION

From hundreds of MHz or more, digital signals begin to behave as waves, so that the PCB (Printed Circuit Board) traces must be designed as transmission lines. The transmission line is characterized by the characteristic-impedance *Z*, which shows the easiness of the signal to transmit. And if some devices or electrical components, which are equivalent to capacitors or inductors, are connected to the transmission line, they become sources of impedance-mismatching, and cause waveform-distortion, or decrease SI (signal integrity) as shown in Fig. 1.

Conventionally, some local-impedance-matching techniques such as SSTL[1] have been used to solve the impedance-mismatching problem. These techniques, however, have not been going well gradually as the frequency increases and approaches to the GHz-region.

In order to overcome this difficulty in the conventional techniques, we have already proposed a novel technique called "Segmental Transmission Line (STL)", and have shown its fundamental effectiveness on some simple transmission models [2][3], where only capacitors are connected. In the high-speed digital-signal transfer, however, not only the capacitances but some inductances, which come from VLSI packages and connectors connected two PCB boards for example, also cause impedance-mismatch and affect the waveform.

In this paper, we apply the STL to the bus system where inductances are also connected to the transmission line as well as the capacitances, and show its effectiveness quantitatively on computer-simulations and actual experiments.

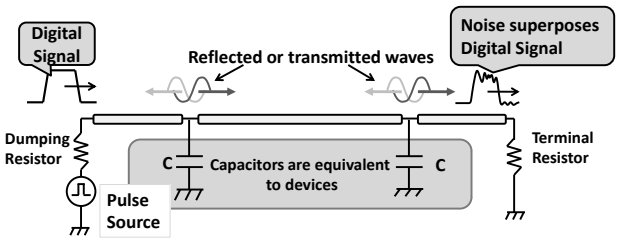

Fig.1 Decline of Signal Integrity

II. SEGMENTAL TRANSMISSION LINE

In order to improve SI in PCB traces, we have already proposed a novel transmission called Segmental Transmission Line (STL) [2]. In the STL, a transmission line is divided into multiple segments of individual characteristic-impedance Z_i and segment-length L_i. In the strip-line structure, or micro-strip line structure in the PCB traces, the characteristic impedance Z is a function of the segment-width W, i.e., $Z=f(W)$. Each segment has thus its own width W_i and length L_i individually as design parameters as shown in Fig.2 if the STL is applied to the PCB trace.

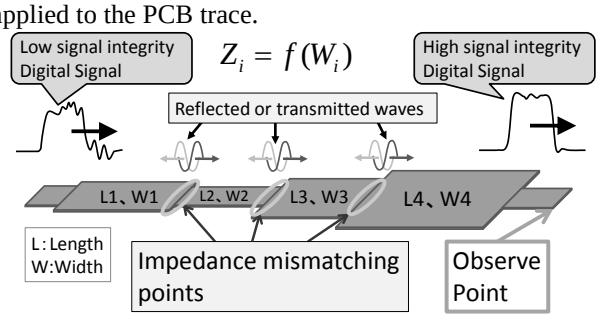

Fig.2 Configuration of Segmental Transmission Line

In the STL, each boundary between adjacent segments causes an impedance-mismatch-point as a matter of course, and reflection waves and transmitted waves occurs at each boundary as a result. In the STL, superposition of the multiple reflection-waves from all boundaries is used to improve the waveform distortion at target points in the transmission line by adjusting W_i and L_i of each segment.

III. GENETIC ALGORITHMS

In the STL, however, there is a troublesome barrier in its design: finding the best combination of all parameters is next to impossible because combinatorial explosion occurs in its search process. Assuming that there are 10 segments, each of which consists of 10 width-candidates and 100 length-candidates, the total number of combinations comes to $(10 \times 100)^{10} = 10^{30}$. This astronomical number prevents us to evaluating all of them in real time. In order to overcome this problem, we apply the genetic algorithms (GA) [4], which is one of optimization algorithms mimicking the biological evolution, to the problem. And more positive reason we use GA is that the STL structure of one dimentional array will be well mapped onto the chromosome stroucure in GA as shown in Fig.3.

Figure 4 shows the flowchart of the STL-design using GA. Genetic operations are executed repetitively until they reach the finish condition. Difference area between the target and the observed waveforms shown in the figure is used to evaluate the chromosome, that is, the reciprocal of the difference area is used as score, or fitness of the chromosome.

IV. EXPERIMENTAL RESULTS

We use a bus-system shown in Fig.5 to evaluate the STL. This bus-system models a transmission line with a Ball Grid Array (BGA) or a Land Grid Array (LGA) connected with it as shown in Fig. 6. There are bunches of boding wires inside the BGA or LGA package, and they need to be considered as inductances as the frequency increases.

1. Simulation Experiments

Figure 7 shows a waveform observed at the observing point in Fig. 5. As shown in Fig. 7, the logic-margins degrease to critical ranges; high-level-logic-margin is 0.3V and low-level-logic-margin is 0.32V. To recover the logic margins, STL is thus applied.

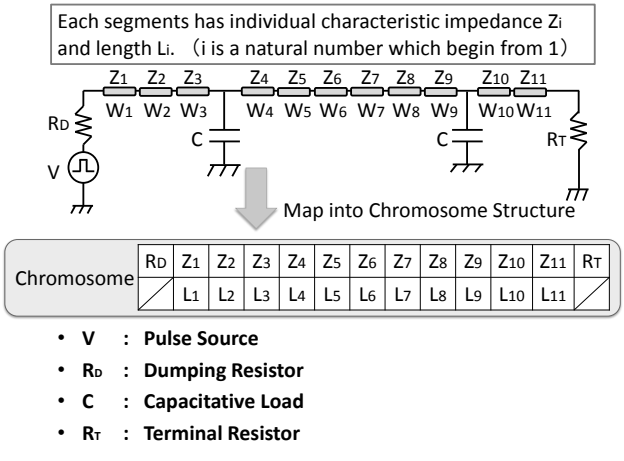

Fig.3 Structure of STL and Chromosome

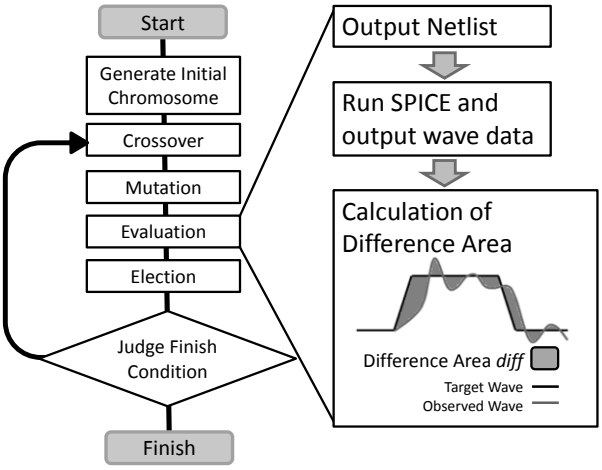

Fig.4 STL-Design Flowchart using GA

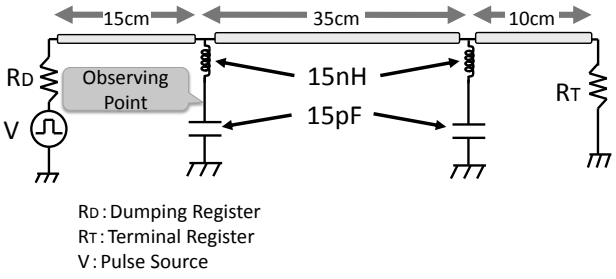

Fig.5 Target Bus-system

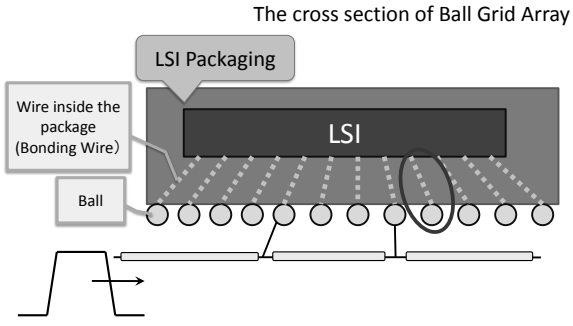

Fig.6 Cross sectional view of Ball Grid Array

Table 1 shows the condition of the STL-Designer using GA, and Fig.8 shows an STL design result for the bus-system including inductances. Figure 9 shows the waveform at the observing point in Fig. 8 in the STL. Both of the high-level-logic-margin and low-level-logic-margin increase to 0.5Vs. Table 2 summarizes the experimental results. High improvement ratios of 1.67 and 1.56 were achieved in high-level-logic-margin and low-level-logic-margin, respectively compared to a conventional transmission line.

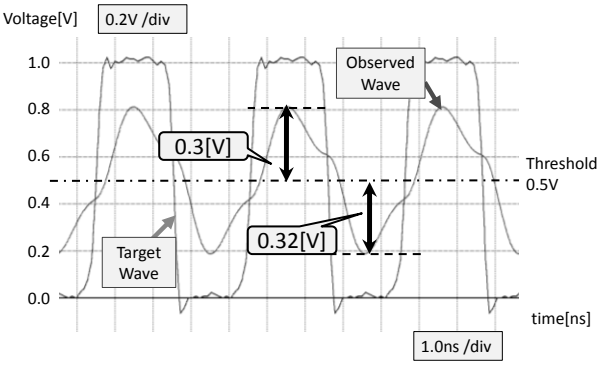

Fig.7 Waveforms of Conventional Transmission Line on Simulations

Table. 1 Conditions of GA

Lengths	15cm,35cm,10cm (Total:60cm)
Fraction of segments	6,7,3
Finish condition	1500 generations

2. Prototype Experiments

We fabricated some PCB prototypes to prove the correctness of the simulation results. Prototype PCB boards are shown in Fig. 10: the upper is a conventional transmission line and the lower is an STL. On the PCBs, chip inductors and chip capacitors are used and soldered as the inductors and capacitors in Figs. 5 and 8.

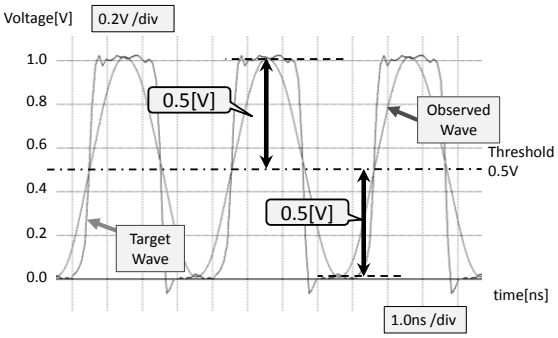

Fig.9 Waveforms of the STL on Simurations

Table. 2 Summary of Simulation Results

	High-level-logic-margin	Low-level-logic-margin
Normal	0.3[V]	0.32[V]
STL	0.5[V]	0.5[V]
Improvement rate	1.67	1.56

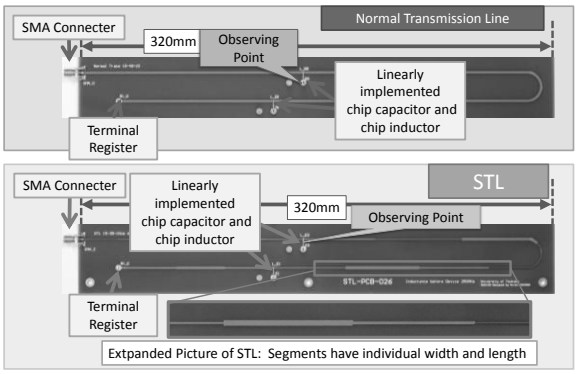

Fig.10 Prototype PCB

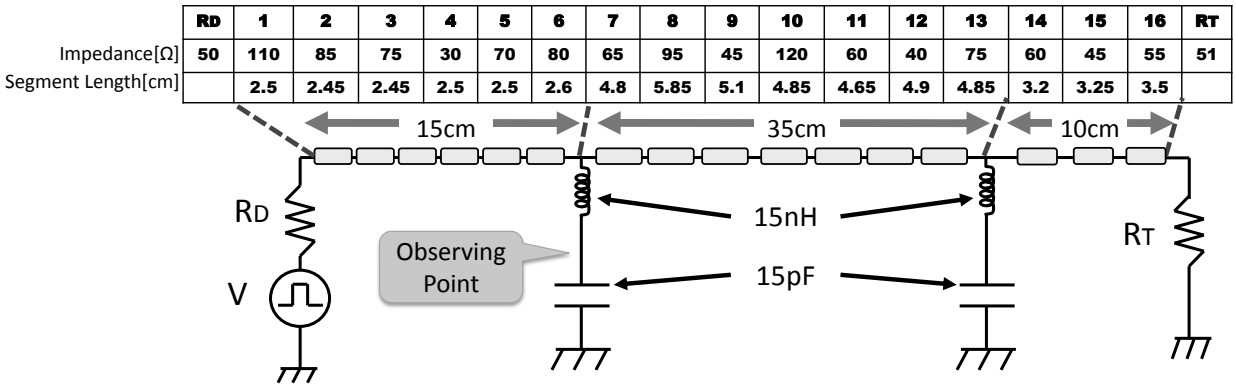

Fig.8 Design Results for STL

Figure 11 shows the measurement environment for the prototype boards. Clock signals are supplied from the pulse generator into the PCBs, and the waveforms are observed using an active probe and a digital sampling oscilloscope.

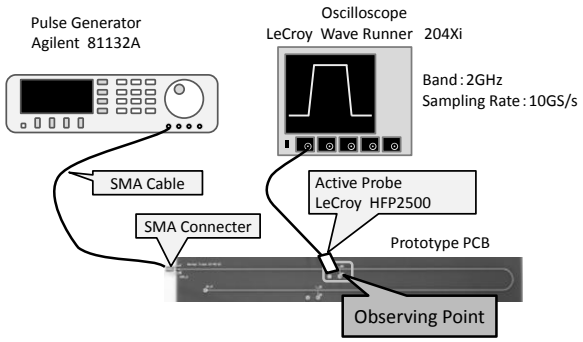

Fig.11 Measurement Environment

Figures 12 and 13 show waveforms in the conventional trace and of the STL, respectively observed with the oscilloscope. Logical margins of 0.34V in high-level and 0.36V in low-level are well improved to 0.52V and 0.5, respectively in the STL.

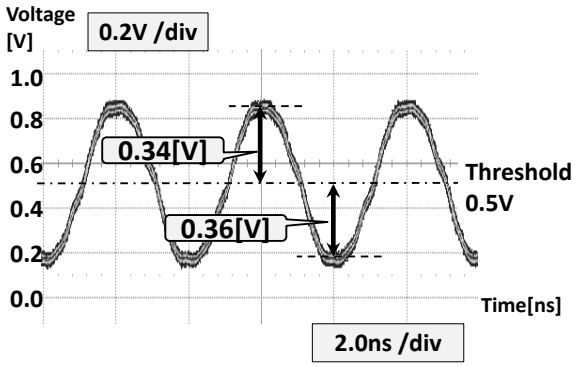

Fig.12 Waveforms observed in Conventional Transmission Line on the Prototype

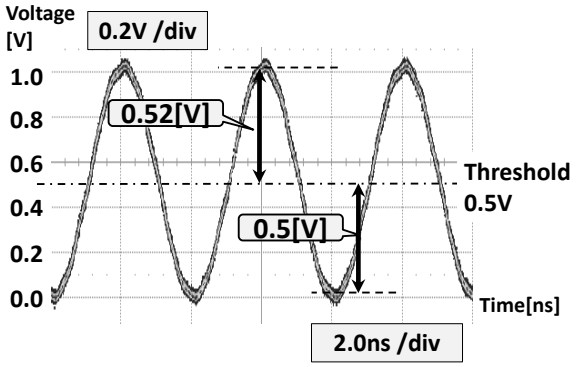

Fig.13 Waveforms observed in STL on the Prototype

Table. 3 Summary of Measurement Results Using Prototype

	High-level-logic-margin	Low-level-logic-margin
Normal	0.34[V]	0.36[V]
STL	0.52[V]	0.5[V]
Improvement rate	1.53	1.39

As the Table. 3 shows, the improvement ratio of high-level-logic-margin is 1.53, and low-level-logic-margin is 1.39. The results indicate that STL is effective to the system which includes inductances directly before the devices.

V. CONCLUSIONS

We newly applied the STL to the bus-system including inductances. The maximum improvement ratio of 1.67 for the distorted waveform in the conventional transmission line was achieved on the computer simulation. We also evaluated the STL using the prototypes, and high improvement rations of 1.53 and 1.39 were achieved in the high-level-logical-margin, and the low-level-logical-margin, respectively. Those results clearly show that the STL is also effective to the bus-system including inductances as well as capacitances.

Our future works is to make clear the differences between simulation and actual experiments. Furthermore, we will also try to make steeper rising/falling waves in the STL.

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