The Sixteenth International Symposium on Artificial Life and Robotics 2011 (AROB 16th '11),
B-Con Plaza, Beppu,Oita, Japan, January 27-29, 2011

A two-variable silicon neuron circuit based on the Izhikevich model

Nobuyuki Mizoguchi, Yuji Nagamatsu, Kazuyuki Aihara, and Takashi Kohno

Institute of Industrial Science, The University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan
(mizoguti@sat.t.u-tokyo.ac.jp)

Abstract: The silicon neuron is an analog electronic circuit that reproduces the dynamics of a neuron. It is a useful element for artificial neural networks that work in real time. Silicon neuron circuits have to be simple and at the same time be able to reproduce rich dynamics in order to reproduce various activities of neural networks with a compact, low-power consumption, and easy-to-configure circuit. We have been developing a silicon neuron circuit based on the Izhikevich model, which has rich dynamics in spite of its simplicity. In our previous works, we proposed a simple and low-power consumption silicon neuron circuit by reconstructing the mathematical structure in the original model using an analog electronic circuit. In this paper, we propose an improved circuit in which all of the MOSFETs are operated in the subthreshold region.

Keywords:Silicon neuron, Izhikevich model, mathematical structure-based method, subthreshold

I Introduction

The dynamics of neurons and that of neural networks have been widely researched. Many mathematical models of neurons have been developed[1, 2, 3] to reconstruct their dynamics and simulations conducted[4, 5, 6] to reproduce various functions of neural networks such as rhythmic movements, associative memory, and pattern recognition. The silicon neuron reproduces the dynamics of a neuron in an electronic circuit. The network of silicon neurons can operate in real time regardless of its size, which is difficult by the simulation using digital computers. In addition, it can be compact if it is implemented into an analog Very Large Scale Integrated circuit (aVLSI). For those reasons, the silicon neuron is expected to be applied for real time systems such as hybrid systems, medical devices, and robots.

Basically, silicon neurons have been developed by two different approaches. The first one is to reproduce only significant neuronal behaviors, which is called the phenomenological method. Silicon neuron circuits designed by this method[7] tend to be simple but can only reproduce a few firing patterns because of its oversimplified dynamics. The second one is to reproduce the neuronal dynamics minutely by solving the ionic conductance models, which is called the conductance based method. Silicon neurons designed by this method[8] can reproduce various firing patterns but their circuitry is complex and large.

Recently, Kohno[9] have proposed another method, the mathematical-structure-based approach, which allows us to design simple circuits with rich dynamics by reproducing the mathematical structure of the original models. By using this method, Nagamatsu[10] proposed a silicon neuron circuit (we call it the previous circuit in this paper) which reproduces the mathematical structure of the Izhikevich model[11]. This silicon neuron circuit reconstructs the dynamics of the original model with a simple circuit whose average power consumption is about 15 nW. However, in the circuit that implements jump of the state in the original model (we call this circuit reset circuit) the voltage variation is relatively large in comparison to other parts of the circuit operated in subthreshold region. Besides this, the input current that triggers spiking of the silicon neuron needs to be considerably small. It is likely to be difficult to produce.

In this paper, we propose an improved circuit with a new reset circuit in which the voltage swing is about 0.4 V, which is lower than that of the previous circuit by about 2.25 V. In addition, we scaled up the input current by altering a part of the circuit. These modifications are expected to lower the difficulty in aVLSI implementation of this circuit.

II Izhikevich model

The Izhikevich model consists of two-variable differential equations with jump of the state:

$$\frac{dv}{dt} = 0.04v^2 + 5v + 140 - u + I \tag{1}$$

$$\frac{du}{dt} = a(bu - v) \tag{2}$$

$$\text{if } \ v = 30\,\text{mV} \ \text{ then } \ v \leftarrow c, u \leftarrow u + d \tag{3}$$

where v and u are the membrane potential and an internal variable respectively. This model can reproduce 20 firing patterns that neurons in the cortical area of the brain exhibit, by tuning the four parameters: a, b, c, and d[12]. The parameter a controls the time constant of u, and b represents the slope of the u-nullcline, the line where the derivative of u is zero, which is shown in Fig. 3(a). The parameters a and b control the characteristics of the equilibrium points where the v-nullcline intersects with the u-nullcline. The parameters c and d respectively determine the membrane potential and the increment of u when a jump of the state occurs. These two parameters mainly control the characteristics of

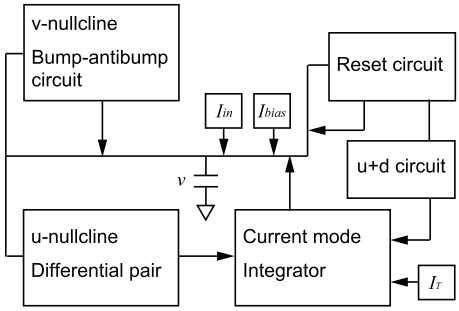


Figure 1: Block diagram of our silicon neuron circuit.

the burst firing.

III Designed circuit

In this section, we show the design of the improved silicon neuron circuit based on the Izhikevich model comparing to the previous one proposed by Nagamatsu[10]. Figure 1 shows the block diagram of our improved circuit.

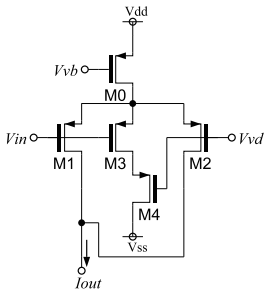
1 Mathematical-structure-based approach

This circuit is designed by using mathematical-structure-based approach proposed by Kohno[9]. In this method, we reconstruct the mathematical structure in the original model using output characteristic curves of simple analog electronic circuits, which allows us to avoid using complex circuits to directly approximate the equations in the original model.

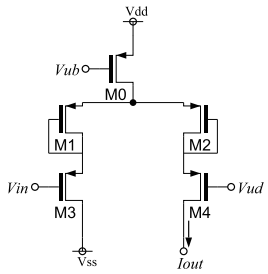
2 Reproducing v- and u-nullclines

To reconstruct the mathematical structure, we reproduced the v- and the u-nullclines by circuits shown in Fig. 2. In the previous circuit, the v-nullcline was reproduced by two differential pair circuits, but in the improved circuit, a bump-antibump circuit[13] is used because it consumes half as much power as the two differential pairs to get the parabolic output current of the same scale. We have increased the bias voltage to scale up the input current that triggers spiking of the silicon neuron, yet the improved circuit consumes as low power as the previous one. It is because the new reset circuit consumes less power than the previous one by about 9 nW. This cancels the increment of the power consumption of the alternative v-nullcline circuit which is about 7 nW. The u-nullcline is reproduced by the same circuit as the previous one: a differential pair circuit with source degeneration.The characteristic curves of the v-nullcline and the u-nullcline circuits are shown in Fig. 3(b) and their theoretical formulae are described in Eqs. (4) and (5) respectively.

$$I_{out} = I_b \left(1 - \frac{1}{1 + \frac{4}{S}\cosh^2 \frac{\kappa(Vin - Vvd)}{2}} \right) \qquad (4)$$

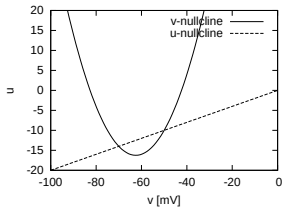


(a)

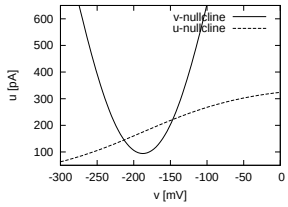


(b)

Figure 2: Schematics of the circuits that produce the nullclines. (a) The bump-antibump circuit that produces the v-nullcline. (b) The degenerated differential pair circuit that produces the u-nullcline.



(a)



(b)

Figure 3: Comparison between the nullclines of the original model and those of our circuit. (a) The v- and the u-nullclines of the original model. (b)Those of our circuit that has the same geometry as the original model even though they don't have exactly the same shape.

$$I_{out} = \frac{I_b}{1 + \exp \frac{-\kappa(Vin - Vud)}{2U_T}} \qquad (5)$$

As shown in Fig. 3(b), the width of the v-nullcline of our circuit is three times as large as that of the original model but it doesn't matter if we scale the membrane potential appropriately. We have to add an amplifier that scales v down to one-third to output the original membrane potential, but there is no need to do so if silicon neurons are interconnected via silicon synapses that reproduce the dynamics of synapses because their circuit can be designed to accept the voltage scale of our silicon neuron circuit. Also, in our circuit the v-nullcline is not exactly parabolic and the u-nullcline not exactly linear but it doesn't matter because it has the same geometrical arrangement as the original one and we can reconstruct the same mathematical structure if we configure the parameters appropriately.

3 Current-mode integrator

A current-mode integrator is used to integrate the equation for the variable u because it is represented by the amount of the current from the capacitance that represents the membrane potential v. Figure 4 shows the current-mode integrator designed to operate in the subthreshold region

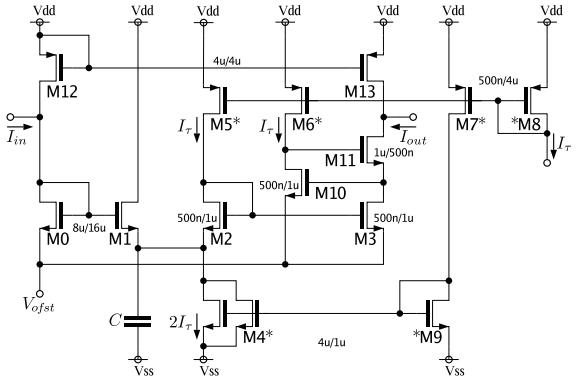


Figure 4: Schematic of the current-mode integrator[14]. I_{out} is temporal integration of $I_{in} - I_{out}$, which represents the variable u. The time constant depends on C and I_τ, which corresponds to the parameter a

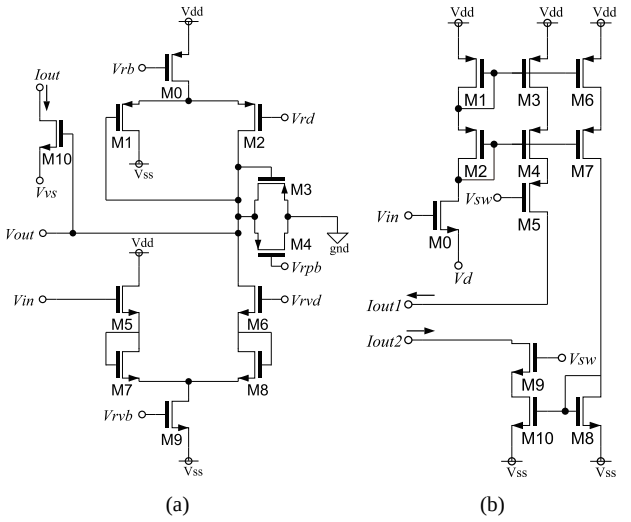


Figure 5: Schematics of the circuits that implement the jumps of the state. (a) The reset circuit that switches v from 90 mV to c mV. Both V_{in} and I_{out} are connected to the capacitance that represents the membrane potential v. V_{out} becomes high while reset operation. (b) The u+d circuit that increases u by d while the reset circuit is switching the value of v. The input voltage V_{in} is connected to V_{out} of the reset circuit. The bias voltage V_{sw} is the switch that shuts off either I_{out1} that represents the positive d or I_{out2} that represents the negative d.

and to be suitable for implementation by relatively fine process such as .35 μm[14]. This circuit implements the integration described as follows:

$$\frac{dI_{out}}{dt} = \frac{I_\tau}{CU_T}(I_{in} - I_{out}) \tag{6}$$

where I_{out} is the output current of the integrator that represents u, I_{in} is the input current that comes from the u-nullcline circuit, C is the capacitance in the integrator, U_T is the thermal voltage, and I_τ is the constant current that represents the parameter a.

4 Reset circuit and u+d circuit

In the previous silicon neuron circuit, the output voltage of the reset circuit swings from -1.65V to 1V when it switches v from 30 mV to c, which is relatively large voltage variation in comparison to the other parts of the circuit operated in subthreshold region. This considerably increases the difficulty in layout mask design and potential troubles in its operation. In the improved circuit, we propose a new reset circuit with a circuit that switches u to u+d (we call it u+d circuit) as shown in the Fig. 5. The reset circuit switches the membrane potential v to c when it exceeds 90 mV (30 mV in the original model). In this operation, the output voltage of our reset circuit keeps high, which makes the u+d circuit increase or decrease the variable u by d. The voltage swing of the output voltage is about 0.4 V, which is lower than that of the previous one by about 2.25 V. The parameter c and d can be configured by the bias voltages V_{rvb} and V_{rvd} in Fig. 5(a) and by V_d in Fig. 5(b) respectively.

5 Bias current that controls the position of v-nullcline

We use the bias current I_{bias} to configure the parameter b as in the previous circuit. Current I_{bias} is injected into or taken up from the capacitor that represents the membrane potential v. In the u-v phase plane, it means I_{bias} moves the v-nullcline up or down and this can configure the characteristics of the equilibrium points as the parameter b in the original model (see Fig. 6).

IV Simulation

We validated our silicon neuron circuit by HSpice circuit simulation using TSMC .35μm CMOS mixed signal process PDK. Vdd and Vss are 1.65V and -1.65V respectively. The simulation results are shown Fig. 7. We have successfully found the parameter voltages for 17 firing patterns out of 20 that the Izhikevich model produces.

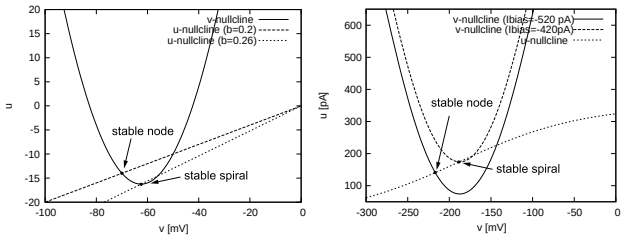


Figure 6: (a) In the original model, the parameter b controls the slope of the u-nullcline. (b) In our circuit, the parameter I_{bias} moves the v-nullcline up and down. The characteristics of the equilibrium points are tuned to be same as in (a).

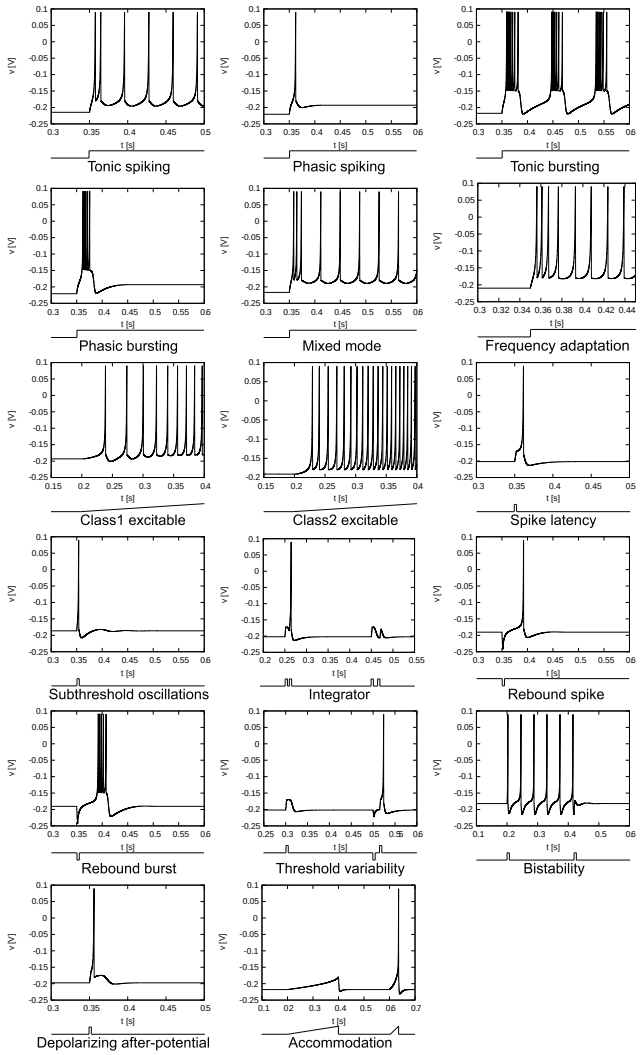


Figure 7: Produced firing patterns.

V Conclusion

We proposed an improved silicon neuron circuit based on the Izhikevich model. The voltage swing of the new reset circuit is about 0.4 V which is smaller than that of the previous circuit by about 2.25 V. In addition, we redesigned the v-nullcline circuit and changed the bias voltages to scale up the input current, yet the improved circuit consumes as low power as the previous one does. These improvements are suitable for aVLSI implementation in which MOSFETs are operated in subthreshold region. We have reproduced 17 firing patterns out of 20 that the Izhikevich model produces.

Acknowledgements

The study was supported by JST PRESTO program and was partially supported by a Grant-in-Aid for Young Scientists (A) 19680015 from the Ministry of Education, Culture, Sports, Science, and Technology, the Japanese Government.

References

[1] A. L. Hodgkin and A. F. Huxley, "A quantitative description of membrane current and its application to conduction and excitation in nerve," The Journal of Physiology, vol. 117, no. 4, pp. 500-544, Aug. 1952.

[2] C. Morris and H. Lecar, "Voltage oscillations in the Barnacle giant muscle fiber," Biophysical Journal, vol. 35, no. 1, pp. 193-213, Jul. 1981.

[3] J. L. Hindmarsh and R. M. Rose, "A model of neuronal bursting using three coupled first order differential equations," Proceedings of the Royal Society B, vol. 221, no. 1222, pp. 87-102, Mar. 1984.

[4] A. A. V. Hill, J. Lu, M. A. Masino, O.H. olsen, R.L. calabrese, "A model of a segmental oscillator in the leech heartbeat neuronal network," J. Comp. Neurosci. 10, 281-302, 2001.

[5] E. M. Izhikevich, "Weakly pulse-coupled oscillators, FM interactions, synchronization, and oscillatory associative memory", IEEE Transactions on Neural Networks, 10, pp. 508-526, 1999.

[6] C. D. Brody, J. J. Hopfield, "Simple networks for spike-timing-based computation, with application to olfactory processing", Neuron 37:843-52, 2003.

[7] G. Indiveri, "A low-power adaptive integrate-and-fire neuron circuit, Circuits and System," 2003. ISCAS '3. Procedings of the 2003 International Symposium, Vol. 4, pp. 820-823.

[8] M. F. Simoni, G. S. Cymbalyuk, and M. E. Sorensen, "A Multiconductance Silicon Neuron With Biologically Matched Dynamics," IEEE Transactions on Biomedical Engineering, Vol.51, No.2, 2004.

[9] T. Kohno and K. Aihara, "A Design Method for Analog and Digital Silicon Neurons -Mathematical-Model-Based Method-," AIP Conference Proceedings, Vol. 1028, pp. 113-128, 2008.

[10] Y. Nagamatsu, K. Aihara, and T. Kohno, "An Izhikevich type silicon neuron circuit," Proceedings of International Symposium on Artificial Life and Robotics 2010, OS4-1, 6th, Feb., 2010.

[11] E. M. Izhikevich, "Simple Model of Spiking Neurons," IEEE Transactions on Neural Networks, Vol. 14, No. 6, November 2003.

[12] E. M. Izhikevich, "Which Model to Use for Cortical Spiking Neurons?," IEEE Transactions on Neural Networks, Vol. 15, No. 5, September 2004.

[13] T. Delbruck, "Bump Circuits," Caltech, Pasadena, CA, Tech. Rep. CNS Memo 26, May 1993.

[14] T. Kohno and K. Aihara, "A simple aVLSI burst silicon neuron circuit," Proceedings of the 2008 International Symposium on Nonlinear Theory and its Applications, pp. 556-559, Sep., 2008.