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A correction circuit of Hall sensor signal base speed measurement for BLDC motors

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Abstract: A speed correction circuit is proposed in this paper, the speed measurement is based on Hall sensor signal. Brushless DC (BLDC) motors are more and more popular, and the Hall sensors are usually built in for commutation. The Hall sensors and poles of the rotor are supposed to be placed in uniform distance and angle, then Hall sensor signal feedbacks are also used to measure motor speed. However, there is misalignment, and what will cause the error of measurement. A method is discussed to estimate the error of misalignment, and the inaccuracy could be corrected by the proposed circuit. This circuit is based on the hardware description language and implemented in FPGA, and then the synthesizing simulation results are presented to prove this circuit is workable.

Keywords: Hall sensor, FPGA, BLDC Motor, misalignment correction.

1 INTRODUCTION

The speed measurement of BLDC motors is usually based on the Hall sensor signals, but there are some errors have to be suppressed. Due to its high power density, easy maintenance and simple driving, BLDC motors are more popular. Although, an accurate rotor encoder is not necessary, to decide the commutation, the rotor position information is still important, and Hall sensors are a regular solution. Basically, the Hall sensor signal feedbacks could be used to measure motor speed, Hall sensors are supposed on uniform distance and the angles of rotor poles are considered as equal. However, there are misalignments for placement of Hall sensors and poles in consumer motors, and the inaccuracy will cause the speed measurement error. For example, for a four poles three phase BLDC motor, the Hall sensor should feedback a new signal in every 30 degree rotation, but the misalignment will cause that the feedback angle is not exactly 30 degree, and include the measurement error. A typical real experimental example is shown in Fig. 1, a motor runs in steady state and MCU clock is captured to calculate motor speed when Hall sensor signal is updated. Here, vertical axis is clock count between every two Hall sensor feedbacks and the waveform is similar to a periodic signal in 12Hz, then period should be caused by the misalignment. Author discussed this phenomenon in Chung-Wen Hung [1], and proposed dynamic moving average filter to get a trade-off between stable and fast response. Samoylenko [2] also proposed different filters and compared the performances. Chung-Wen Hung [1] and N. Samoylenko[2] treated the variation of Hall sensor feedback intervals caused by unbalance placement of Hall sensors and poles as noise, then designed a suitable filter to get correct signal. Neither required hardware circuit, but both took CPU calculation resource and induced phase delay.

P.B. Beccue [3] discussed a compensation method that implemented a Hall effect position observer to estimate the rotor position. This method used the angle and axes to define the rotor position and based on those to build a table. And it used the table to compute the error of the rotor angle and compensate the phase of the rotor.

S.-Y. Kim [4] intro- deuced a vector-tracking observer that used a feed forward input of the average rotor speed to calculate the rotor speed. And this observer is utilized to obtain the phase detector, which is used to estimate the angle error of the rotor. Using the observer to estimate the back-EMF and compare with the reference back-EMF to define the position and implement the compensation. Anno Yoo [5] used the d-q axis to define the phase and current, and utilized the dual observer to estimate rotor speed and position, respectively. Based on the rotor position to obtain the error value and implemented the compensation algorithm. Kuang-Yao Cheng [6] implemented a mixed mode integrated circuit (IC) of the sensorless commutation for BLDC motor. This circuit utilized the back-EMF and zero-crossing point to detect the phase error. Compensation the phase error by the rotor speed estimation depended on the changing phase lag due to the low-pass filtering of the terminal voltages. The said compensation methods have to implement the complex observer and the other Hall sensor detection circuit to perform the estimator.

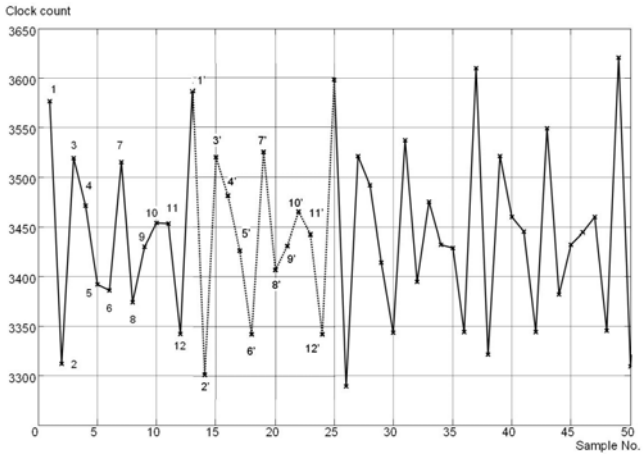

Fig. 1. The intervals of the Hall sensor updating

This paper presents a speed correction circuit for a HALL sensor signal base. This circuit is implemented in hardware description language and on filed programming gate array (FPGA), and it could calibrate the speed measurement what is caused by the misalignment of the poles of the rotor and Hall sensors. A method is discussed to estimate the error of misalignment, and the circuit structure will be introduced. Then, the synthesizing simulation results are presented to prove this circuit is workable

2 A CORRECTION OF HALL SENSOR SIGN AL BASE SPEED MEASUREMENT

Normally, the Hall sensor feedback will be used to measure motor speed if Hall sensors are build-in for commutation, and the sequence is depend on rotate direction as shown in Fig. 2. The change of the Hall sensor signal means that the rotor rotated 60 degree for 2-pole, or 60 degree for 4-pole motor. Next, the time interval between two signal changing could be measured to calculate motor speed. The speed correction method and circuit are also depended on the information of Hall sensor signals and time intervals.

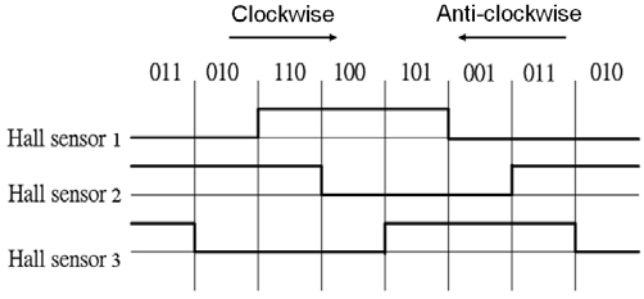

Fig. 2. The intervals of the Hall sensor updating

2.1 A calibration method of Hall sensor signal base speed measurement

A calibration method [1] is discussed to get more accurate speed estimation based on Hall sensors. To get the error ration of every sector caused by misalignments of Hall sensors and rotor poles, the motor could be driven by another constant speed motor or fixed PWM duty to free, and get every sectors average speed error ratios. The correction of speed would be based on these error ratios. As shown in Fig. 3, a zoom figure of Fig. 2, and the average clock count of a 3-phase 4-pole BLDC motor is about 3390, and the clock count samples is corrected by the error ratio and shows more accurate results. Note, in Fig. 3, the samples is a periodic signal with the period of twelve samples caused by the sensor and pole misalignments, however, the correction is indexed in only 6 Hall sensor signal and only 6 correction ratio could be used. The R.M.S. of error is reduced less than 40% of original's. If this method is used in a 2 pole BLDC motor, the effect should be better.

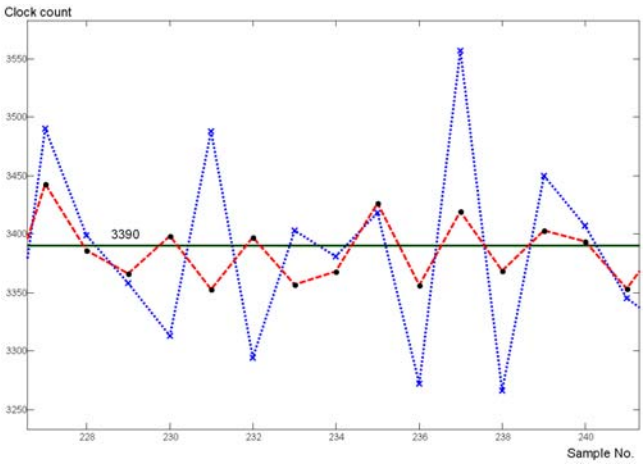

Fig. 3. The average (solid), sampling (dot) and correction (dash) clock count

2.2 A Correction circuit of Hall sensor signal base s peed measurement

Based on above discussion, a correction circuit is proposed to implement the algorithm. The system block diagram is shown in Fig. 4: there are three one-bit inputs for Hall sensor signals, six register inputs for correction ratios and clock; one output is the interrupt to inform the controller to read the new 16 bits corrected time interval and update the speed calculation.

The clock source is connected to the controller or MCU system clock, it is much faster than Hall sensor changing, and then the clock could be used to latch the Hall sensor signals. A previous Hall sensor capture is applied to latch the last the Hall sensor status, and the previous and current Hall sensor statuses are send to a compare block. When the Hall signals in two capture registers are different, an interrupt signal is declared to indicate that the rotor already rotes over a new sector, 30 or 60 degree, and the controller could get new speed measurement and change the commutation status. This interrupt signal is also used to latch the content of the clock counter into correction block, which counter is used to accumulate the clock in a sector, then the counter is reset to zero for next new sector. The signal of the previous Hall sensor capture register is employed to index the corresponding correction ratio from

the six correction registers, which contents are got based on correction method what is discussed in last section. Note, to use the previous Hall sensor signal to select correction register is better than the current signal, and it could ignore the direction of a motor because it is the previous sector could be corrected. If the current Hall sensor signal is used to index, the direction should be consider in the structure and circuit would be more complicated.

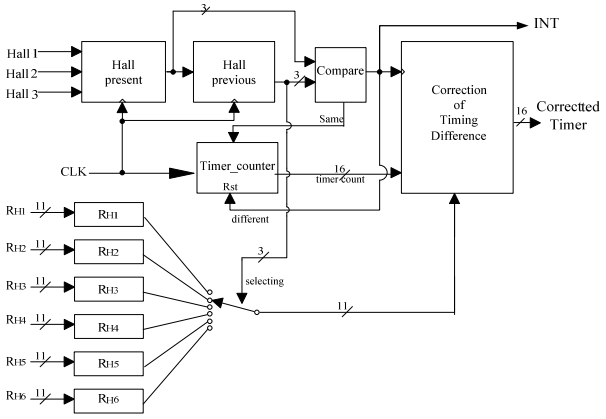

Fig. 4. The block diagram of HALL sensor signal base speed measurement

3 Hardware Implementation and Simulation Results

3.1 Hardware implementation

The structure is implemented in verilog HDL and on FPGA, Altera Cyclone II EP2C70: 176 logic elements, 63 registers and 2 embedded multiplier 9-bit elements are used. The bit width of timer counter is set to 16 bits, what is depend on clock source and lowest speed motor, means the clock number between two Hall sensor changes, and the correction ratio registers are set to 11 bits for the fraction format.

For reduction of circuit the complexity, the number format should be fixed pointed. The number correction ration is in the quasi positive I1Q10 mode, due to that the error ranges are about 15% which means correction ration is a fraction number from 0.85 to 1.15. Every correction number is multiplied with 1024 before written into the register. When interrupt occurs, the product of clock counting and correction ratio is right shifted by 10 bits, then fraction effect is achieved.

Table 1. Correction ratios

Hall sensor Index	Correction Ratio
100	1.00 = 10000000000 B
110	0.95 = 01111001100 B
010	1.05 = 10000110011 B
011	1.10 = 10001100110 B
001	0.97 = 01111000011 B
101	0.93 = 01101110101 B

3.2 Simulation Results

The simulation results are shown in this section to presented workability of the proposed structure. The values of correction ratios are list in table 1, what includes Hall sensor index, fraction mode ratios and I1Q10 mode ratios. The function is verified by Fig. 5. The clock is set on 100M Hz, 10 nS, and Hall sensor signal changes every 511 clock cycles. The output 485 is the product of 511 and correct ratio of a110, because the correction ration is indexed by previous Hall sensor signal "110", which ration is 0.95. Next out put is 511, due to previous index is 100. The simulation result shows the structure works well.

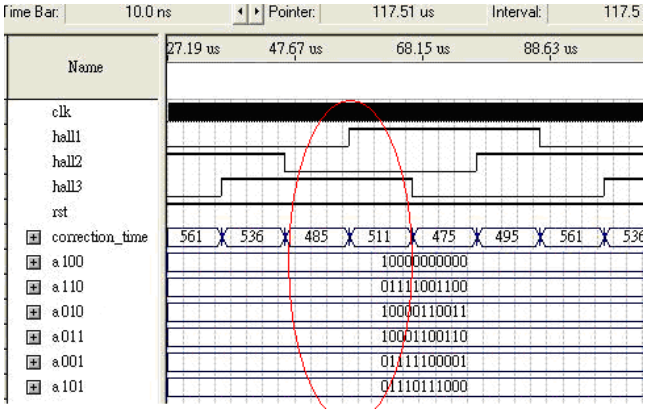

Fig. 5. The simulation results of fixed Hall sensor intervals

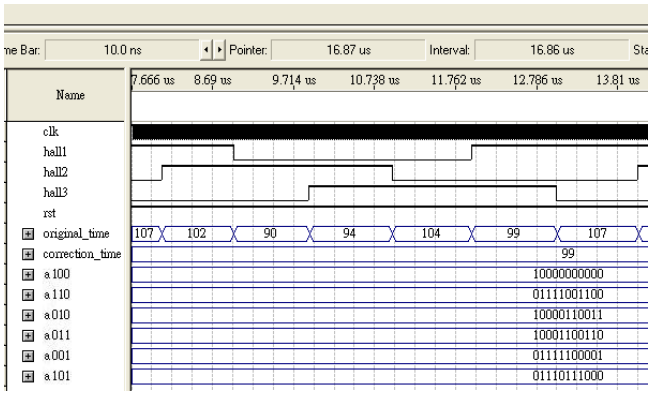

Fig. 6. The simulation results of variable Hall sensor intervals of misalignment

To get more detail simulation result, the Hall sensor intervals are set similar to real misalignments, and the counter will catch the different intervals corresponded with Hall sensor sectors. The result is present in Fig. 6, the timer counter before correction and correction output are probed. All of outputs are 99 cycles; no matter counter is capture 107 or 90. For example, when the content of counter is 90, the previous Hall sensor signal is "011", which indicates that correction ration is 1.10, and the corrected output is 99 cycles. Again, for the 107 output, the previous index is "101" and the ration is 0.93, so, the output should be 99. Note, to get more accurate result, 512 is added to product before shift to perform rounding.

4 CONCLUSION

A correction circuit of speed measurement what is based on Hall sensor signals for BLDC motors is proposed this paper. The Hall sensors are originally built in for commutation in BLDC motors, and normally there are misalignments in the placement of sensors and rotor poles in consumer motors due to cost issue. To get accurate speed, FPGA is used to implement a correction circuit, the correction ratios are prepared in the calibration processor, then a corresponding ratio what is index previous Hall sensor signal multiplier with the content of timer counter what is rest every Hall sensor changes. The simulation results show the structure is work successfully, and could provide more accurate speed measurement. Moreover, the resource requirement of the circuit is few and could be implemented easily to improve the performance of a BLDC motor system.

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