The Seventeenth International Symposium on Artificial Life and Robotics 2012 (AROB 17th '12),
B-Con Plaza, Beppu, Oita, Japan, January 19-21, 2012

Binary MEMS optically reconfigurable gate array for an artificial brain system

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Abstract: Optically reconfigurable gate arrays (ORGAs) consisting of a holographic memory, a laser diode array, and a programmable gate array were developed to realize an artificial brain system for robots. In the ORGA, much information or many reconfiguration contexts can be stored in a volume-type holographic memory and can be programmed dynamically onto a programmable gate array at nanosecond-order perfectly in parallel. Therefore, by exploiting the huge storage capacity of the holographic memory and large parallel operations on a programmable gate array, huge parallel brain operations can be executed quickly on an ORGA. This paper presents a proposal of a binary MEMS-interleaving reconfiguration operation on an optically reconfigurable gate array for an artificial brain system.

Keywords: Field programmable gate arrays, optically reconfigurable gate arrays, programmable logic devices.

1 INTRODUCTION

An adult human brain holds more than 100 billion neurons and more numerous synapses connecting them [1]–[3]. To realize an artificial neural network system that can provide performance similar to that of a human brain, a huge number of parallel operations must be executed on an embedded system. In this case, a three-dimensional very large scale integration (VLSI) technology is one candidate.

However, fortunately, the response time of each neuron of a human brain is about 1,000,000 times slower than that of the currently available VLSIs. Therefore, for emulation of a human brain, one neuron circuit can serve 1,000,000 neuron operations. Despite that rapid performance, since the storage capacity and bandwidth of synaptic connections of a human brain are extremely large and broad, respectively, the capabilities of current silicon memories remain insufficient to emulate synaptic weights.

Holographic storage systems are excellent candidates for such human brain systems since three-dimensional holographic memories can easily provide large storage capacity. The density potential reaches V/λ^3, where V denotes the recording volume and λ is the wavelength of the recording light source [4][5]. For example, photorefractive crystal holographic memories $LiNb0_3$ can store 100 bits/μm^2 [6] and can achieve 100 Gbit/in^2 [7]. The area densities are superior to even the latest 32 nm process dynamic random access memory (DRAM) cell with area of 0.039 μm^2 [8].

To date, optically reconfigurable gate arrays (ORGAs) have been developed to realize next-generation large-virtual gate count programmable VLSIs [9]–[12]. An ORGA typically comprises an ORGA-VLSI, a holographic memory, and a laser array. The ORGA-VLSI is a fine-grained gate array, as are field-programmable gate arrays (FPGAs)[13],[14]. Its function is the same as those of currently available FPGAs, but the ORGA-VLSI configuration procedure is executed optically. In an ORGA, many configuration contexts can be stored on a holographic memory that is addressed by a laser array, and which can be implemented dynamically onto the ORGA-VLSI in a very short time [11]. By virtue of those features, the ORGA can achieve numerous virtual gates along with a high-speed nanosecond-order context switching capability. Using these features, vastly numerous synaptic weight operations and neuron operations can be executed. However, although the ORGA architecture presents such advantages, an important issue is its future mass production. The salient cost problem is posed by the laser array. For example, to implement a million reconfiguration contexts onto an ORGA, a million lasers must be implemented onto the ORGA, but a laser array with numerous lasers is invariably expensive. In contrast, other components such as photopolymer holographic memory materials and a standard process ORGA-VLSI are cheap. Therefore, the number of lasers presents an important concern in developing ORGAs.

Recently, a useful microelectromechanical system (MEMS) technology, a digital micromirror device (DMD), was produced by Texas Instruments Inc. [15],[16]. The specifications of a DMD device are presented in Table 1. A photograph of the chip, which consists of 1,024 $\times$ 768 mirrors, is portrayed in Fig. 1. Potentially, it can address numerous reconfiguration contexts. Although the response time of the DMD device is slow, many interleaving methods have been proposed to increase the speed of slow response devices, particularly the speed of memory devices [17]–[20].

Therefore, this paper presents a proposal of a binary

Table 1. Specifications of a digital mirror array device.

	0.55 XGA
Resolution	1024 × 768 mirros
Mirror tilt angle	±12°
Mirror size	10.8 μm × 10.8 μm
Package size (inch)	1.6 × 1.25

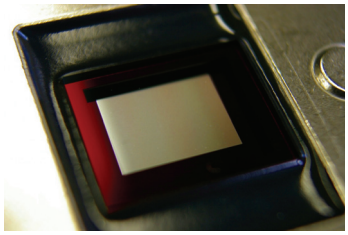


Fig. 1. Photograph of the digital mirror array device.

MEMS optically reconfigurable gate array for use in an artificial brain system based on a binary MEMS-interleaving method.

2 BINARY MEMS-INTERLEAVING METHOD

2.1 MEMS device

As explained previously, the MEMS device described in Table 1 and presented in Fig. 1 has 1,024 × 768 tiny mirrors, each having a size of 10.8 × 10.8 μm^2. For example, if the DMD device is implemented and each mirror is used for addressing one configuration context, then 786,432 configuration contexts can be addressed. Therefore, the MEMS is useful for addressing numerous reconfiguration contexts. However, the microsecond-order switching of the MEMS device is not sufficiently fast. In artificial brain operations on an ORGA, the gate array must be reconfigured at nanosecond-order. Therefore, microsecond-order switching speed is insufficient for an artificial brain system.

2.2 Interleaving method

This paper therefore presents a proposal of a binary MEMS-interleaving ORGA designed to achieve a higher reconfiguration frequency than the MEMS switching speed. Up to now, many interleaving methods have been proposed in earlier reports of the literature [17]–[20]. Based on them, the MEMS - laser addressing interleaving method concept was produced. A block diagram of a novel concept of a MEMS-interleaving ORGA is depicted in Fig. 2. In this method, some MEMS mirrors and a laser are grouped to a module, as shown in Fig. 3. In addition, many modules are implemented onto a MEMS-interleaving ORGA. When a certain reconfiguration request arises, firstly, a MEMS mirror angle is changed and then a laser in the same module turns on

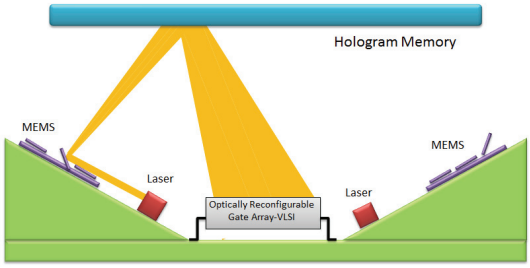


Fig. 2. Novel concept of a MEMS-interleaving optically reconfigurable gate array (ORGA).

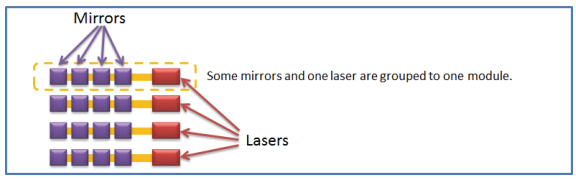


Fig. 3. Laser-MEMS module.

so that the laser beam is reflected on the MEMS mirror and is incident to a holographic memory. Then, an optical configuration context is read out from the holographic memory and finally, the configuration context is programmed onto an ORGA-VLSI, as shown in Fig. 2. This is a normal reconfiguration procedure. Of course, if a second configuration procedure is executed inside the same module, then the procedure must wait until the first mirror angle is changed to an off state, another mirror angle is changed to an on-state, and the laser turns on again. In this case, the wait period becomes the summation of the MEMS response time and the laser switching period. Consequently, the period of this reconfiguration procedure is longer than the MEMS switching period: no acceleration can be achieved.

However, using the interleaving method, in such a case, a laser of another module, for which the angles of mirrors have already been adjusted and a configuration procedure has been readied, turns on. Furthermore, the lasers on the third module, the fourth module, and so on turn on in sequence. While the other modules function, modules which have completed one configuration procedure start to prepare the next-configuration mirror position. For example, it is assumed that if the respective switching speeds of a laser and MEMS are 10 ns and 10 μs, and 1001 modules which have 1000 mirrors are implemented onto the ORGA, then the ORGA has a million configuration contexts. Each reconfiguration can be executed within 10 ns constantly because mirrors of the idle module can be changed for 10,000 ns while another 1000 modules work for a period 1000 × 10 ns. Therefore, using this method, even a million configuration contexts can be switched by only 1001 lasers.

Up to now, a MEMS-interleaving read operation of a holo-

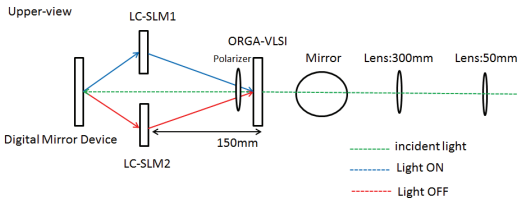


Fig. 4. Experimental system.

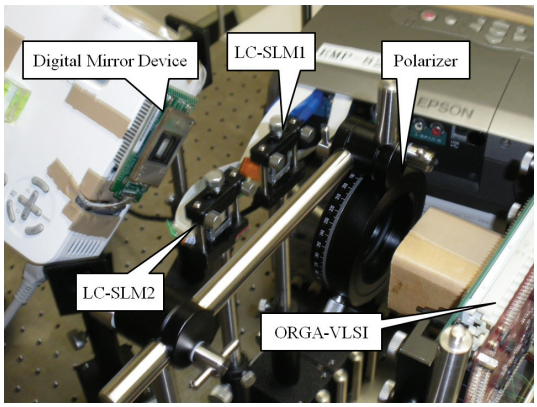
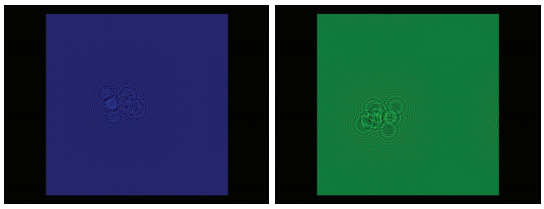


Fig. 5. Photograph of the experimental system.

graphic memory, which can control a MEMS mirror as an ON/OFF switch, has been proposed [21]. In this method, 1000 mirrors could only address 1000 configuration contexts. However, if we can use both angles of ON state and OFF state of each mirror for configurations, the number of mirrors can also be decreased. Therefore, this paper proposes a binary MEMS-interleaving method. In this method, a mirror is used to generate two beams instead of ON/OFF states. Therefore, 1000 mirrors address 2000 reconfiguration contexts. Results show that this system uses fewer lasers and fewer MEMS mirrors.

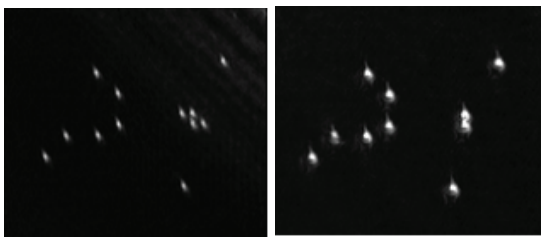
3 EXPERIMENTAL SYSTEM

For this study, a single-module implementation with two configuration contexts was conducted as the first step for binary MEMS-interleaving ORGA development. Figures 4 and 5 respectively portray a block diagram and a photograph of the binary MEMS-interleaving ORGA. The binary MEMS-interleaving ORGA was constructed by using a 532 nm, 300 mW laser (torus 532; Laser Quantum), a MEMS device, two liquid-crystal spatial light modulators (LC-SLMs), and an ORGA-VLSI. The 1.7-mm-diameter beam from the laser source was expanded six times to 10.2 mm using two lenses of 50 mm focal length and 300 mm focal length. The expanded beam is incident to a MEMS mirror device (Digital Mirror Device). In this case, the mirror state is controlled as with a binary state. If the MEMS mirror is +12°, then the reflected laser beam is incident to the LC-SLM1, which



(a) OR circuit (b) AND circuit

Fig. 6. Holographic memory patterns calculated using a personal computer.



(a) OR circuit (b) AND circuit

Fig. 7. CCD-captured images of configuration context patterns of an OR circuit and an AND circuit.

functions as a holographic memory. However, the reflected laser beam is incident to the LC-SLM2 if the MEMS mirror is -12°. Two holographic memory patterns respectively recording an OR circuit and an AND circuit were calculated as shown in Figs. 6(a) and 6(b) and were displayed on LC-SLM1 and LC-SLM2, respectively. Holographic memory patterns comprised 700 × 700 pixels. The LC-SLMs are a 90° twisted nematic device with a thin film transistor. Each pixel is 12 μm × 12 μm. The first holographic memory pattern shown in Fig. 6(a) is used for +12°-state of a MEMS mirror and the second holographic memory pattern shown in Fig. 6(b) is used for -12°-state of the MEMS mirror. For this implementation, an ORGA was placed 150 mm distant from the LC-SLM. The ORGA had been fabricated using a 0.35 μm triple-metal CMOS process. Photodiodes were constructed between the N-well layer and the P-substrate. The photodiode size and distance between photodiodes were designed as 25.5 × 25.5 μm^2 and as 90 μm to facilitate the optical alignment. The gate array structure is fundamentally identical to that of typical FPGAs. The ORGA-VLSI chip includes 4 logic blocks, 5 switching matrices, and 12 I/O bits. In all, 340 photodiodes were used to program the gate array.

4 EXPERIMENTAL RESULTS

Using the optical system explained above, the binary MEMS-interleaving operation has been confirmed. First, the MEMS mirror angle was adjusted to +12°. Then a laser source was turned on. In this case, the laser beam is reflected on the MEMS mirror. It is then incident to the LC-

SLM1 including a holographic memory pattern of an OR circuit. Finally, the configuration context pattern generated from the holographic memory, as shown in Fig. 7(a), was programmed correctly onto an ORGA-VLSI. For the next experiment, the MEMS mirror angle was adjusted to -12°. Then a laser source was turned on. In this case, the laser beam is reflected on the MEMS mirror. It is incident to the LC-SLM2, including a holographic memory pattern of an AND circuit. Finally, the configuration context pattern generated from the holographic memory pattern shown in Fig. 7(b) was programmed correctly onto an ORGA-VLSI. Therefore, we have demonstrated that one MEMS mirror can address two configuration contexts.

5 CONCLUSION

Optically reconfigurable gate arrays (ORGAs) have been developed to realize artificial brain systems for robots. Nevertheless, conventional ORGAs require many lasers to address the configuration contexts stored on a holographic memory. Such laser arrays with numerous lasers are invariably expensive, which presents an extremely important concern related to their development. Therefore, to address numerous configuration contexts with fewer lasers, this paper has proposed a novel method using a binary MEMS-interleaving ORGA. If a 4,000 × 4,000 mirror array with 10 μs response time can be used along with about 1,000 lasers that can generate a 10 ns light pulse, then 32 million reconfiguration contexts can be achieved along with 10 ns reconfiguration speed, since two configuration contexts can be addressed by a MEMS mirror. This method can be expected to provide an addressing capability of a billion configuration contexts along with nanosecond-order high-speed configuration capability which is very suitable for emulation of an artificial neural network.

ACKNOWLEDGMENTS

This research was supported by the Accelerating Utilization of University Intellectual Property Program. The VLSI chip in this study was fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Co. Ltd. and Toppan Printing Co. Ltd.

REFERENCES

[1] Antonio R. Damasio et al., "The Scientific American Book of the Brain," New York: Scientific American, 1999.

[2] A. L. Hodgkin, A. F. Huxley, "A quantitative description of membrane current and its application to conduction and excitation in nerve," Journal of Physiology, vol 117, pp. 500-544, 1952.

[3] R. H. Adrian, "Conduction Velocity and Gating Current in the Squid Giant Axon," Proceedings of the Royal Society B: Biological Sciences, vol. 189, pp. 81-86, 1975.

[4] P. J. van Heerden, "Theory of optical information storage in solids," Applied Optics, vol. 2, 393–400 (1963).

[5] T. Watanabe, M. Watanabe, "Robust holographic storage system design," Optics Express, Vol. 19, No. 24, pp. 24147-24158, Nov., 2011.

[6] A. Pu and D. Psaltis, "Holographic data storage with 100 bits/μm^2 density," Optical Data Storage Topical Meeting Conference Digest, 48–49 (1997).

[7] G. W. Burr, C. M. Jefferson, H. Coufal, C. Gollasch, M. Jurich, J. A. Hoffnagle, R. Macfarlane, and R. M. Shelby, "Volume holographic data storage at an areal density of 100 Gbit/in^2," Conference on Lasers and Electro-Optics, 188–189 (2000).

[8] N. Butt et al., "A 0.039 μm^2 High Performance eDRAM Cell based on 32nm High-K/Metal SOI Technology," IEEE International Electron Devices Meeting, 27.5.1 – 27.5.4 (2010).

[9] N. Yamaguchi, M. Watanabe, "Liquid crystal holographic configurations for ORGAs," Applied Optics, Vol. 47, No. 28, pp. 4692-4700, 2008.

[10] D. Seto, M. Watanabe, "A dynamic optically reconfigurable gate array - perfect emulation," IEEE Journal of Quantum Electronics, Vol. 44, Issue 5, pp. 493-500, 2008.

[11] M. Nakajima, M. Watanabe, "A four-context optically differential reconfigurable gate array," IEEE/OSA Journal of Lightwave Technology, Vol. 27, No 20, pp. 4460-4470, 2009.

[12] M. Nakajima, M. Watanabe, "A 100-Context Optically Reconfigurable Gate Array," IEEE International Symposium on Circuits and Systems, pp. 2884-2887, 2010.

[13] Altera Corporation, "Altera Devices," http://www. altera.com.

[14] Xilinx Inc., "Xilinx Product Data Sheets," http://www. xilinx.com.

[15] Texas Instruments, "DLP," http://www.ti.com/

[16] Texas Instruments, "Discovery 4000," http://www.ti.com/

[17] B. Khargharia, S. Hariri, M.S. Yousif, "An Adaptive Interleaving Technique for Memory Performance-per-Watt Management," IEEE Transactions on Parallel and Distributed Systems, Vol. 20, Issue 7, pp. 1011 - 1022, 2009.

[18] G.S. Sohi, "High-bandwidth interleaved memories for vector processors-a simulation study," IEEE Transactions on Computers, Vol. 42, Issue 1, pp. 34 - 44, 1993.

[19] C. Song; A. Postula, "Synthesis of custom interleaved memory systems," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, Issue 1, pp. 74 - 83, 2000.

[20] T. VanCourt, M.C. Herbordt, "Application-Specific Memory Interleaving Enables High Performance in FPGA-based Grid Computations," IEEE Symposium on Field-Programmable Custom Computing Machines, pp. 305-306, 2006.

[21] H. Morita, M. Watanabe, "MEMS interleaving read operation of a holographic memory for optically reconfigurable gate arrays," International Workshop on Applied Reconfigurable Computing, Lecture Notes in Computer Science, Vol. 6578, pp. 242-252, 2011.