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Parallel Turing Machines on Four-Dimensional Input Tapes

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Abstract

A parallel Turing machine (PTM) proposed by Wiedermann is a set of identical usual sequential Turing machines (STM's) cooperating on two common tapes − storage tape and input tape. On the other hand, due to the advances in many application areas such as motion picture processing, computer animation, virtual reality systems, and so forth, it has become increasingly apparent that the study of four-dimensional pattern has been of crucial importance. Thus, we think that the study of four-dimensional automata as a computational model of four-dimensional pattern processing has also been meaningful. In this paper, we propose a four-dimensional parallel Turing machine (4-PTM), and investigate its some properties, based on hardware complexity.

Key Words: computational complexity, four-dimensional automaton, hardware-bounded computation, parallel Turing machine, space constructibility

1 Introduction

Informally, a parallel Turing machine (PTM) is a set of identical sequential Turing machines (STM's) cooperating on two common tapes − storage tape and input tape [6]. Moreover, STM's which represent the individual processors of the parallel computer can multiply themselves in the course of computation. In [6] it is shown, for example, that every PTM can be simulated by an STM in polynomial time, and that the PTM cannot be simulated by any sequential Turing machine in linear space.

In [1,2], two- or three-dimensional version of PTM was investigated. On the other hand, due to the advances in many application areas such as motion picture processing, computer animation, and so forth, it has become increasingly apparent that the study of four-dimensional pattern processing has been of crucial importance. Thus, we think that the study of four-dimensional automata as a computational model of four-dimensional pattern processing has also been meaningful. During the past about seven years, automata on a four-dimensional tape have been proposed and several properties of such automata have been obtained . In this paper, we propose a four-dimensional parallel Turing machine (4-PTM), and investigate its some properties. Especially, we deal with a hardware-bounded 4-PTM, a variant of the 4-PTM, which each side-length of each input tape is equivalent.

2 Preliminaries

Definition 2.1. Let Σ be a finite set of symbols, a *four-dimensional tape* over Σ is a four-dimensional rectangular array of elements of Σ. The set of all four-dimensional tapes over Σ is denoted by $\Sigma^{(4)}$. Given a tape $x \in \Sigma^{(4)}$, for each integer j $(1 \leq j \leq 4)$, we let $l_j(x)$ be the length of x along the jth axis. The set of all $x \in \Sigma^{(4)}$ with $l_1(x) = n_1$,$l_2(x) = n_2$,$l_3(x)=n_3$ and $l_4(x)=n_4$ is denoted by $\Sigma^{(n_1,n_2,n_3,n_4)}$. When $1 \leq i_j \leq l_j(x)$ for each j $(1 \leq j \leq 4)$, let $x(i_1, i_2, i_3, i_4)$ denote the symbol in x with coordinates (i_1, i_2, i_3, i_4). Furthermore, we define

$$x[(i_1, i_2, i_3, i_4),(i'_1, i'_2, i'_3, i'_4)],$$

only when $1 \leq i_j \leq i'_j \leq l_j(x)$ for each integer j $(1 \leq j \leq 4)$, as the four-dimensional input tape y satisfying the following conditions:

(1) for each j $(1 \leq j \leq 4)$, $l_j(y) = i'_j - i_j + 1$;

(2) for each r_1, r_2, r_3, r_4 $(1 \leq r_1 \leq l_1(y)$, $1 \leq r_2 \leq l_2(y)$, $1 \leq r_3 \leq l_3(y)$, $1 \leq r_4 \leq l_4(y))$, y $(r_1,r_2,r_3,r_4) = x$ $(r_1+i_1\text{-}1,\ r_2+i_2\text{-}1,\ r_3+i_3\text{-}1,\ r_4+i_4\text{-}1)$. (We call $x[(i_1, i_2, i_3, i_4),(i'_1, i'_2, i'_3, i'_4)]$ the $[(i_1, i_2, i_3, i_4),(i'_1,i'_2, i'_3, i'_4)]$-*segment* of x.)

Definition 2.2. *Four-dimensional parallel Turing machine* (denoted by 4-PTM) is a 10-tuple $M = (Q, E, U, q_s, q_0, \Sigma, \Gamma, F, \delta_n, \delta_f)$, where

(1) $Q = E \cup U \cup \{q_0\}$ is a finite set of *states*;

(2) E is a finite set of *nondeterministic states*;
(3) U is a finite set of *fork states*;
(4) q_s is the *quiescent state*;
(5) $q_0 \in Q$ - $\{q_s\}$ is the *initial state*;
(6) Σ is a finite *input alphabet* ($\# \notin \Sigma$ is the *boundary symbol*);
(7) Γ is a finite *storage tape alphabet* containing the special *blank* symbol B;
(8) $F \subseteq Q - \{q_s\}$ is the set of *accepting states*;
(9) $\delta_n : E \times (\Sigma \cup \{\#\}) \times \Gamma \to 2^{(Q-\{q_s\})\times(\Gamma-\{B\})\times D_{in}\times D_s}$ (where D_{in} = {east, west, south, north, up, down, future, past, no move} and D_s = {left, right, no move}) is a *next nondeterministic move function*; and
(10) $\delta_f : U \times (\Sigma \cup \{\#\}) \times \Gamma \to \cup_{1\leq k\leq\infty}((Q-\{q_s\})\times(\Gamma-\{B\})\times D_{in}\times D_s)$ is a *next fork more function* with the restriction that for each $q \in U$, each $a \in \Sigma \cup \{\#\}$, and each $A \in \Gamma$, if $\delta(q,a,A) = ((p_1,c_1,d_{11},d_{21}), (p_2,c_2,d_{12},d_{22}), \ldots, (p_k,c_k,d_{1k},d_{2k}))$, then $c_1 = c_2 = \ldots = c_k$.

As shown in Figure.1, M has a read-only four-dimensional rectangular input tape with boundary symbols "#'s", and one semi-infinite storage tape (extended to the right), initially filled with the blank symbols. Furthermore, M has infinite processors, $P_1, P_2, \ldots$, each of which has its input head and storage-tape head. M starts in the situation that (1) the processors P_1 is in the initial state q_0 with its input head on the upper northwestmost corner of the first cube of the input tape and with its storage-tape head on the leftmost cell of the storage tape, and (2) each of other processors is in the quiescent state q_s with its input head on the upper northwestmost corner of the first cube of the input tape and with its storage-tape head on the leftmost cell of the storage tape.

Seven-way four-dimensional parallel Turing machine (denoted by $SV4\text{-}PTM$) is a 3-PTM, input heads of whose processors cannot move in the past direction. In this paper, we are concerned with three-dimensional parallel Turing machines, which each side-length of each input tape is equivalent. Let $L : \mathbf{N} \to \mathbf{N}$ and $H : \mathbf{N} \to \mathbf{N}$ be functions. A 4-PTM ($SV4\text{-}PTM$) M is called $L(n)$ *space-bounded* if for any $n \geq 1$ and for any input tape x with $l_1(x) = l_2(x) = l_3(x) = l_4(x) = n$, M on x uses at most $L(n)$ cells of the storage tape, and M is $H(n)$ *hardware-bounded* if for any $n \geq 1$ and for any input tape x with $l_1(x) = l_2(x) = l_3(x) = l_4(x) = n$, M on x activates at most $H(n)$ processors. We use the following notations:

· $D4\text{-}PTM(L(n), H(n))$: the class of sets of four-dimensional tapes accepted by $L(n)$ space-bounded and $H(n)$ hardware-bounded deterministic 4-PTM's.

· $N4\text{-}PTM(L(n), H(n))$: the class of sets of four-dimensional tapes accepted by $L(n)$ space-bounded and $H(n)$ hardware-bounded nondeterministic 4-PTM's.

· $DSV4\text{-}PTM(L(n), H(n))$: the class of sets of four-dimensional tapes accepted by $L(n)$ space-bounded and $H(n)$ hardware-bounded deterministic $SV4$-PTM's.

· $NSV4\text{-}PTM(L(n), H(n))$: the class of sets of four-dimensional tapes accepted by $L(n)$ space-bounded and $H(n)$ hardware-bounded nondeterministic $SV4$-PTM's.

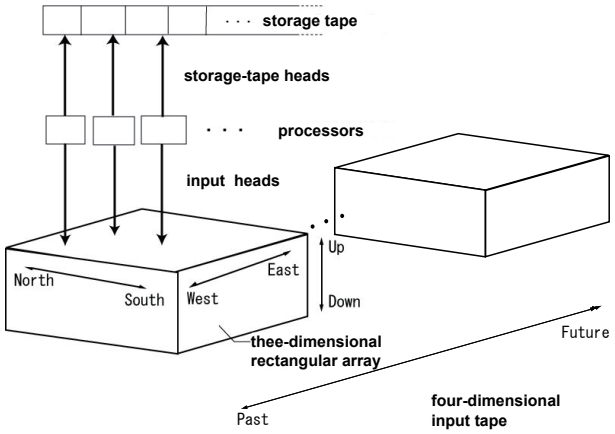

Figure 1: Three-dimensional parallel Turing machine.

3 Main Results

This section mainly investigates accepting powers of $SV4\text{-}PTM$'s, based on hardware complexity.

A function $L : \mathbf{N} \to \mathbf{N}$ is *fully space constructible* by a *k head one-dimensional deterministic Turing machine* if there is a k head one-dimensional deterministic Turing machine [5] M such that for any $n \geq 1$ and any input word x of length n, M on x marks off exactly $L(n)$ cells of the storage tape and halts. (In this case, we say that M *constructs* the function L.)

Theorem 3.1. Let $H : \mathbf{N} \to \mathbf{N}$ *be a function which satisfies the following* (1), (2), and (3), where $k \geq 1$ *is an integer*:

(1) *H is fully space constructible by a k head one-dimensional deterministic Truing machine*;
(2) $\exists_{n_0} \in \mathbf{N}$, $\forall_n \geq n_0$ $[H(n) \geq k]$;
(3) $\binom{H(n)}{2} \leq \frac{n}{2} (n \leq 2)$.
Furthermore, let $H' : \mathbf{N} \to \mathbf{N}$ *and* $L : \mathbf{N} \to \mathbf{N}$ be functions which satisfy the following (4) and (5):
(4) $\exists_{n_0} \in \mathbf{N}$, $\forall_n \geq n_0$ $[\binom{H'(n)}{2} \leq \binom{H(n)}{2}]$;
(5) $\max \{ H'(n)^2 \binom{H(n)}{2} log\, n,$
$H'(n)^2 \binom{H(n)}{2} log\, L(n),$
$L(n) H'(n) \binom{H(n)}{2} \} = o(n)$.
Then,
$DSV4\text{-}PTM(H(n),H(n)) - NSV4\text{-}PTM(L(n), H'(n)) \neq \phi$.

Proof: Let $T(H)$ be the following set depending on the function H in the theorem:

$T(H) = \{ x \in \{0,1\}^{(4)} \mid \exists_n \geq 2 \binom{H(n)}{2}$ $[l_1(x)=l_2(x) =l_3(x)=l_4(x)=n$ & $\forall_i (1 \leq i \leq \binom{H(n)}{2})$ [the ith cube of x is identical with the $(2\binom{H(n)}{2}+1-$i)th cube of x]] $\}$.

To prove the theorem, we show that $T(H) \in DSV4\text{-}PTM\ (H(n), H(n)) - NSV4\text{-}PTM\ (L(n), H(n))$. $T(H)$ is accepted by an $H(n)$ space-bounded and $H(n)$ hardware-bounded $DSV4\text{-}PTM$ M which acts as follows. Suppose that an input tape x with $l_1(x) = l_2(x) = l_3(x) = l_4(x) = n$ is presented to M. Let M_1 be a k head one-dimensional deterministic Turing machine which constructs the function H. By simulating the action of M_1 on the first cube of x, the first k processors $P_1, P_2, \ldots, P_k$ of M mark off exactly $H(n)$ cells of the storage tape.

After this, each processor $P_i (2 \leq i \leq k)$ positions its storage-tape head on the ith cell (from the left) of the storage tape, and processor P activates processors $P_{k+1}, P_{k+2}, \ldots, P_{H(n)}$ in such a way that for each j $(k+1 \leq j \leq H(n))$, the storage-tape head of P_j is positioned on the jth cell (from the left) of the storage tape. Then P_1 positions the input head at the northwestmost corner of the $(2\binom{H(n)}{2} + 2 - H(n))$th cube of x, which for each i $(2 \leq i \leq H(n))$, P_i positions the input head on the northwestmost corner of the $(H(n) - i + 1)$th cube of x. And P_1 systematically traverses the $(2\binom{H(n)}{2} + 2 - H(n))$th cube, ..., the $2\binom{H(n)}{2}$th cube (from the first plane to the last plane in each cube, from the first column to the last column in each plane, and from the first row to the last row in each column), and compares these cubes with the $(H(n)-1)$th cubes, ..., the first cubes, respectively, by using the information from $P_2, P_3, \ldots, P_{H(n)}$.

These input heads are then positioned at the northwestmost end of the $H(n)$th cube of x. The same procedure is used inductively to verify that $H(n)$th cube through the $(2\binom{H(n)}{2} + 1 - H(n))$th cube has a desired form.

Next, we show that $T(H) \notin NSV4\text{-}PTM$ $(L(n), H'(n))$. Suppose to the contrary that there is an $NSV4\text{-}PTM$ $(L(n), H'(n))$ M' accepting $T(H)$. Let s and t be the numbers of states of the finite control of each processor and storage tape symbols of M', respectively. For large $n \geq 2\binom{H(n)}{2}$, let

$V(n) = \{ x \in \{0,1\}^{(4)} \mid l_1(x) = l_2(x) = l_3(x) = l_4(x) = n$ & $\forall_i (1 \leq i \leq \binom{H(n)}{2}))$ [the ith cube of x is identical with the $(2\binom{H(n)}{2} + 1 - i)$th plane of x] & $[(1,1,1,2\binom{H(n)}{2}+1), (n,n,n,n)] \in \{0\}^{(4)} \}$.

Below, we consider the computation of M' on input tapes in $V(n)$. Clearly, each tape x in $V(n)$ is in $T(H)$, and so x is accepted by M'.

A configuration of M' is an infinite-tuple $(\alpha, ((h_1,k_1,j_1,i_1),q_1,r_1), ((h_2,k_2,j_2,i_2),q_2,r_2), \ldots, ((h_m,k_m,j_m,i_m), q_m, r_m), \ldots)$ where α is the non-blank contents of the storage tape of M', and for each $m \geq 1$, (h_m,k_m,j_m,i_m), q_m and r_m are the input head position, the state of the finite control and the position of storage-tape head of the mth processor of M', respectively. The type of a configuration $C=(\alpha, ((h_1,k_1,j_1,i_1),q_1,r_1), ((h_2,k_2,j_2,i_2),q_2,r_2), \ldots, ((h_m,k_m,j_m,i_m), q_m, r_m), \ldots)$, denoted by $Type(C)$, is an infinite-tuple $([i_1], \ldots, [i_m], \ldots)$, where for each $m \geq 1$,

$$[i_m] = \begin{cases} i_m & \text{if } i_m \leq \binom{H(n)}{2} \\ 2\binom{H(n)}{2} & otherwise. \end{cases}$$

Let $c_1(x)$, $c_2(x)$, ..., $c_{l_x}(x)$ be the sequence of configurations of M' during an (arbitrary selected) accepting computation of M' on a tape x in $V(n)$. Here l_x is the length of this computation. Let $d_1(x), d_2(x), \ldots, d_{l'x}(x)$ be the subsequence obtained by selecting $c_1(x)$ and all subsequent $c_i(x)$'s such that $Type(c_i(x)) \neq Type(c_{i+1}(x))$. We call $d_1(x), d_2(x), \ldots, d_{l'x}(x)$ the pattern of x. Let $p(n)$ be the number of possible pattern of M' on x in $V(n)$. Since $L'_x \leq H'(n)(2\binom{H(n)}{2} - 1) + 1 \equiv Q(x)$ (note that M' uses at most $H'(n)$ processors when it reads tapes in $V(n)$), we get the following inequality:

$p(x) \leq ((s(n+1)(n+1)(n+1)(n+1)L(n))^{H'(m)t^{L(n)}})^{Q(n)}$.

Now we classify the tapes in $V(n)$ according to their patterns. There must exist a pattern $\hat{d}_1, \hat{d}_2, \ldots, \hat{d}_l$ which corresponds to a set $S(n)$ of at least $2^{n \times n \times n \times n \times \binom{H(n)}{2}} / p(n)$ tapes in $V(n)$. Since $\binom{H'(n)}{2} \leq \binom{H(n)}{2}$ (from condition (4) in the theorem), the same observation as in the proof of Theorem 3 in [3] reveals that for any computation of M' on an $x \in V(n)$, there exists an index i

such that the ith cube of x and the $(2\binom{H(n)}{2}+1-i)$th cube of x are never being read simultaneously.

Let i_0 be such a value for the pattern $\hat{d}_1, \hat{d}_2, \ldots, \hat{d}_l$. we now define a binary relation E on tapes in $S(n)$ as follows: For each u and v in $S(n)$, let

${}_uE_v \Leftrightarrow \forall_i(\notin \{i_0, i_0, i_0, 2\binom{H(n)}{2}+1-i_0)$ [ith cubes of u and v are identical].

Obviously the relation E is an equivalence relation, and there are $q(n) = 2^{n^3(\binom{H(n)}{2}-1)}$ E-equivalence classes of tapes in $S(n)$. From condition (5) in the theorem, we can easily show that $|S(n)| > q(n)$ for large n. Therefore, there exist two different tapes in $S(n)$ which belong to the same equivalence class. Let x and y be such two different tapes in $S(n)$. And let z be the tape obtained from x by replacing the $(2\binom{H(n)}{2}+1-i_0)$th cube with the $(2\binom{H(n)}{2}+1-i_0)$th cube of y. By an argument similar to that in the proof of theorem 1 in [7], it can be shown that there is an accepting computation of M' on z. Consequently, z must be accepted by M'. This contradicts the fact z is not in $T(H)$. □

We consider the following functions:

· $log^{(1)}n = \begin{cases} 0 & (n=0) \\ \lceil logn \rceil & (n \geq 1), \end{cases}$

and for each $r \geq 1$,

· $log^{(r+1)}n = log^{(1)}(log^{(r)}n)$.

It is shown in [4] that the function $log^{(k)}n$ $(k \geq 1)$ are fully space-constructible by three head one-dimensional deterministic Turing machines. A similar result is provided about the four dimensions. From this fact and Theorem 3.1, we have:

Corollary 3.1. *For each* $k \geq 3$,
$DSV4\text{-}PTM$ $(log^{(k)}n, log^{(k)}n)$ $-$ $NSV4\text{-}PTM$ $(log^{(k)}n, log^{(k+1)}n) \neq \phi$.

Corollary 3.2. *For each* $X \in \{D, N\}$ and each $k \geq 3$,
$XSV4\text{-}PTM$ $(log^{(k)}n, log^{(k+1)}n) \subseteq XSV4\text{-}PTM$ $(log^{(k)}n, log^{(k)}n)$.

Letting $H(n) = k+1$ (where k is a positive integer), $H'(n) = k$, and $L(n) = o(n)$ in Theorem 3.1, we have :
$DSV4\text{-}PTM$ $(k+1, k+1)$ $-$ $NSV4\text{-}PTM$ $(0(n), k)$ $\neq \phi$.

From this and from the obvious fact that

$DSV4\text{-}PTM$ $(k+1, k+1) = DSV4\text{-}PTM(1, k+1)$,

we have the following corollary.

Corollary 3.3. *For any integer* $k \geq 1$,
$DSV4\text{-}PTM$ $(1, k+1)$ $-$ $NSV4\text{-}PTM$ $(o(n), k) \neq \phi$.

4 Conclusion

This paper investigated fundamental properties of four-dimensional parallel Turing machines with bounded number of processors. We conclude the paper by giving several open problems.

(1) What is a relationship between the accepting powers of $SV4\text{-}PTM$'s and $4\text{-}PTM$'s?

(2) What is a hierarchy of the accepting powers of $SV4\text{-}PTM$'s, based on the hardware complexity depending on the side-length of input tapes?

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