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A digital spiking silicon neural network

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Abstract: A silicon neuron is an electrical circuit that replicates the electrophysiological phenomena of biological neural system. Despite most of conventional spiking silicon neuron models are designed for analog circuit technology, we proposed, in the previous study, a digital spiking silicon neuron (DSSN), which is optimally designed for digital circuit technology. The DSSN model was based on a mathematical-modeling point of view and successfully produced three types of neural excitability with fewer hardware resources. In addition to the DSSN, we propose here a digital silicon synapse that mimics the elemental features of a chemical synapse and underlies the construction of a silicon neural network. We built a fully-connected digital silicon neural network with the digital silicon synapses and demonstrate synchronization and phase-locking in neural activities in a hardware description language (HDL) simulation.

Keywords: silicon neural network, digital synaptic circuit

I. INTRODUCTION

The silicon neural network is an electrical circuit that mimics electrophysiological properties and functions of biological neural systems. Such neural system attracts much attention due to not only clinical objectives but also engineering purposes, and their parallel structure and robustness might bring high scalability and adaptability in information processing. Silicon neural networks with these features are applicable to, for example, a real-time simulator of complicated nerve systems [1], a hybrid system of biological and silicon neurons for the purpose of verification of a neuron model [2], and brain machine interfaces.

In the present study, we focused on designing the silicon spiking neural network with DSSNs and the silicon synapses. Spikes (or action potentials) are thought to be a main carrier of information in neural systems and are generated when a neuron receives inputs from other neurons and its membrane potential reaches the threshold. Once a spike is generated, the spike travels to other neurons and yields current on their membrane via excitatory or inhibitory synapses. These synaptic interactions lead variety of neural dynamics. For example, in mutually connected neurons with excitatory synapses, their neural activities tend to be synchronized. Synchronized neural activities are widely observed in biological systems and are supposed to play crucial roles e.g. in cardiac pacemaker cells [3] and in motor controls [4]. Those dynamical features of spiking neural network might bring variety of engineering applications.

In designing the silicon neural network, selection of a proper model is a key issue. One possible approach of neural modeling is to focus on the detail of neurons' structure, for example, multi-compartmental models of neurons based on dynamics of various kinds of ionic channels and dendritic tree structure. Such physiologically realistic neuron models might produce the detail of the neural activity. However, implementations of those models require vast hardware and power resources, and when trying to operate the neural system it can be hard to analyze their behaviors. Another approach is to simplify the neuron model and to optimize them to a target device maintaining the core features of activity of the original neuron. The DSSN model proposed in our previous study is based on this requirement and on mathematical modeling point of view. The DSSN model exhibits rich dynamical behavior and allows us to realize a silicon neural network with fewer hardware resources.

In this paper, we report a digital synaptic circuit with same design principal as that of the DSSN model and a digital silicon neural network with the synaptic circuit. In the following sections, dynamical properties of the DSSN are briefly reviewed. Then, models of synaptic circuits and the neural network are explained. In the result section, phase-locking phenomena of neural activities in the network are demonstrated. In the final section, conclusions, discussions for the result, and our future works are remarked.

II. MODEL AND METHOD

In this study, we used the DSSN model as an element of the neural network, which is optimally designed for digital circuit technology [5] and is described by the following equations:

$$\frac{dv}{dt} = \frac{\phi}{\tau}(f(v) - n + I_0 + I_{stim}) \ , \qquad (1)$$

$$\frac{dn}{dt} = \frac{1}{\tau}(g(v) - n) \ , \tag{2}$$

$$f(v) \equiv \begin{cases} a_n (v + b_n)^2 - c_n & (v < 0) \\ -a_p (v - b_p)^2 + c_p & (v \geq 0) \end{cases} \ , \tag{3}$$

$$g(v) \equiv \begin{cases} k_n (v - p_n)^2 + q_n & (v < r) \\ k_p (v - p_p)^2 + q_p & (v \geq r) \end{cases} \ , \tag{4}$$

where variables v and n respectively represent the membrane potential and an activity of slow ionic channels. Parameters a_x, b_x, c_x, k_x, p_x, q_x (for x=n and p), and r determine dynamical properties of the neuron. Φ and τ are parameters that specify the time constant. I_0 is a constant bias current. I_{stim} is the sum of currents given by other neurons. See reference [5] for the parameter values.

This neuron model is designed so that they can be implemented on limited resource of digital arithmetic circuits while maintaining the qualitative structure of their dynamical system. The structure of the dynamical system can be depicted on the phase-plane plots and the bifurcation diagrams (Fig. 1(a)-(c)). Those plots show structures of dynamics in two different types of neuron models: Class I and II excitability. This classification is based on difference on the frequency-input relationship of a neuron as depicted in Fig. 1(d). A neuron with Class I excitability begins to fire gradually at arbitrarily low frequency as the sustained stimulus current is increased. In Class II excitability, on the other hand, a neuron starts to fire at non-zero frequency. Differences of those excitabilities can be clear with the phase plane and the bifurcation diagrams. In the former, the structure of the dynamical systems are characterized with nullclines, which are sets of points satisfying $\dot{v} = 0$ or $\dot{n} = 0$, called the v- and the n-nullclines respectively. Intersections of these nullclines represent equilibriums whose stabilities are determined by the eigen value analyses. As the magnitude of the input increases, the v-nullcline moves upward in Fig. 1(a) and the position and presence of intersections can be changed as in Fig. 1(b) and (c). In the case of a Class I neuron, the qualitative change in the dynamical system is induced by a saddle-node on invariant circle bifurcation. In a Class II neuron, this is by the Hopf bifurcation.

In order to construct a silicon neural network with DSSNs, we have developed a digital silicon synapse. We used a synaptic model which is analogue to elemental features of activities in biological synapses. The activity of the model synapse is triggered by an arrival of a spike and decays exponentially toward zero [7]. The synaptic model used in this paper is described by

$$\frac{ds}{dt} = -\frac{1}{\tau_s} s + (s_{peak} - s)\delta(t - t_s) \ , \tag{5}$$

where s is a synaptic activity, parameter s_{peak} = 2 is the peak value of synaptic activity, τ_s= 3.2ms is the decay

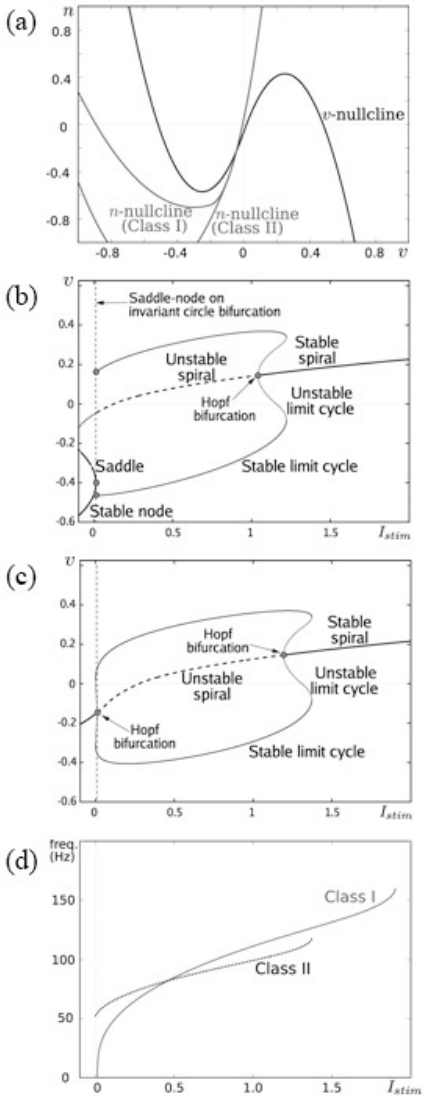

Fig. 1. Analyses of Class I and II neurons in our DSSN model. (a) The *v*-*n* phase plane. (b), (c) Bifurcation diagrams of Class I and II neurons, respectively. (d) Frequency-input relationship of Class I and II neurons. These figures are cited from [5][6].

time constant of synaptic activity, t_s is the time when the presynaptic neuron emits a spike. δ is Dirac's delta function. The second term in the right-hand side of Eq. (5) represents reset of synaptic activity.

Although, a single neuron sends spikes to multiple neurons and generates synaptic currents on their membranes, we assumed that the time series of the synaptic currents are common among these synapses except for their amplitude. In other words, the synaptic currents are given by a product of the synaptic activity and a weight value that corresponds to efficiency of each synapse (Fig. 2).

Figure 3 shows the block diagram of the single spiking neuron circuit and the corresponding synaptic circuit. Three variables in this model, v, n, and s are stored in register circuits (boxes of the right side in Fig. 3) and are updated with difference equations that

are derived from Eqs. (1), (2), and (5). Differences are calculated according to the stored values of the variables and the external input (boxes of the left side in Fig. 3) and these differences are summed with the current states of variables in adders (middle in Fig. 3). The summed values are read out by the variable registers simultaneously at the rising edge of the clock signal. The variable that represents the synaptic activity is reset to their peak value when the sign bit of variable v is switched from 1 to 0, namely, when the membrane potential go through the threshold v=0 from below to above.

As to the network, we constructed a fully-connected network in which all neurons have connections for all other neurons including themselves. In this study, we built a neural network that consists of three silicon neurons connected each other via the silicon synapses of unique weight value w.

In this digital silicon neural network, the variables in above equations are represented by two's complement representation and the size of the circuit is crucially depended on the selection of their bit width. We tried several values for the bit width and found that 19 bit is sufficient to attain accurate integration to operate the silicon neural network appropriately. Furthermore, several parameter values in above models

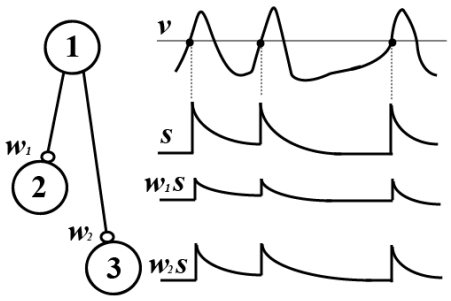

Fig. 2. Schematics of synaptic activity. v represents the membrane potential of neuron 1. s represents a synaptic activity. w_1 and w_2 represent weights of synapses from neuron 1 to neuron 2, and to neuron 3, respectively.

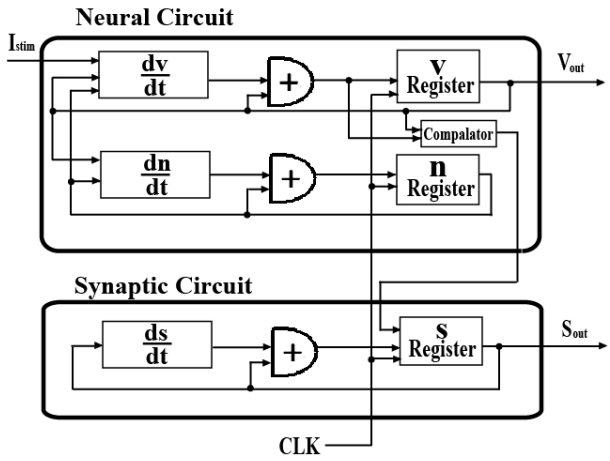

Fig. 3. Block diagram of a single neuron circuit and a synaptic circuit. I_{stim} is the external input. V_{out} is the output of membrane potential. S_{out} is the synaptic activity.

are selected from m th power of two (m is supposed to be an integer number) so that the multiplier circuits can be replaced by bit shifters. This replacement leads remarkable reduction in hardware resource requirement and less latency. In the calculating process of division of τ, bit shift operation is also utilized. We simulated this spiking silicon neural network with a HDL simulator software (Modelsim Xilinx Edition-III). In the following HDL simulation, we set the bit width of variables to be 19 bits.

III. RESULT

We confirmed that the individual spiking silicon neurons show both of Class I and II excitabilities in HDL simulation (Fig. 4). In the Class I mode, our silicon neuron begins to fire at very low frequency and their frequency is gradually increased by an increase in the input magnitude. In the case of the Class II mode, as the input magnitude increased, their frequency suddenly increases just above a threshold and then they increases relatively slowly in the above threshold. In relation to synaptic activity, as the membrane potential exceeds the threshold, synaptic activities are triggered and decayed exponentially.

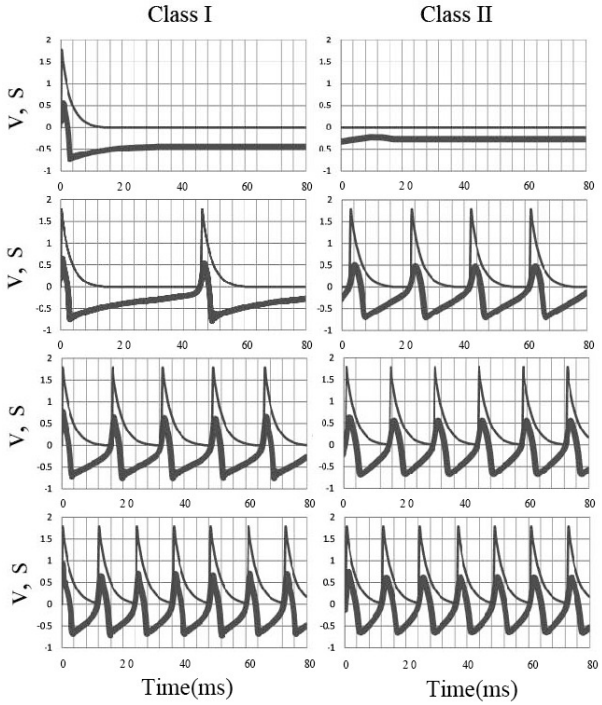

Fig. 4. HDL simulation of our silicon neuron circuit. The vertical axes represent the magnitude of v and s, and these figures show time series from 0 to 80ms. A synaptic activity is indicated by thin curve. The membrane potential is represented by bold curves. The left column is Class I neuron. The right one is Class II neuron. In sequence from top figures, I_{stim}= −0.25, 0.0156, 0.5, 1. Note that in this simulation, the frequencies of v at the values of each I_{stim} about both Class I and II are different from those of Fig. 1(d). However, the qualitative characteristic of Class I and II corresponds to that of Fig. 1(d).

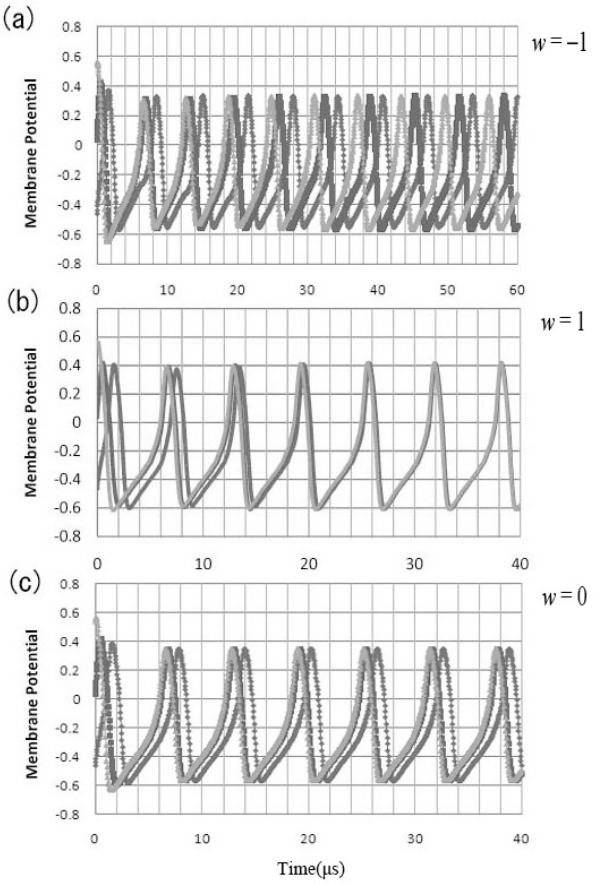

Fig. 5. Responses on the digital silicon neural network. The vertical axes represent the magnitude of *v*. (a) An anti-phase locking. (b) Synchronization. (c) Response without interactions.

As shown in Fig. 5, the spiking silicon neural network shows synchronization and phase-locking phenomena in their activity. We performed simulation for the cases of the inhibitory, excitatory, and neutral synaptic connections. In this simulation, the Class I neurons are implemented. In the model, interaction with inhibitory synapses leads an anti-phase locking (Fig. 5(a)) and excitatory interactions bring the synchronized activities (Fig. 5(b)). These well-ordered collective behaviors cannot be observed without any interactions (Fig. 5(c)).

IV. DISCUSSION AND CONCLUSION

In this paper, we proposed a digital silicon neural network and confirmed, in HDL simulations, that individual neurons show two different classes of excitability and their activities trigger synaptic activities, and that the fully-connected neural network shows synchronization and phase-locking phenomena due to the interaction via the synaptic connection.

In our silicon neural network, several spatio-temporal patterns are realized by changing the connectivity among the network. Application of this phenomenon involves, for example, a control of multi-channel actuators. As the future works, we will implement the silicon neural network in a field programmable gate array (FPGA) and evaluate their performances in such applications. Furthermore, to implement learning ability or flexible plastic features in the silicon neural network, a synaptic plasticity circuit is required. We will develop the plasticity circuit based on the same design principal as used in the present research.

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