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An Izhikevich type silicon neuron circuit

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Abstract: The Izhikevich model is 2-variable differential equations of a qualitative neuron model. In spite of its simple mathematical structure, it can produce a variety of firing patterns because of its nonlinearity, including jump of state in the equations. When we construct spiking neural networks, we need simple circuitry that can produce rich dynamics because more dynamical patterns are thought to give the higher probability of complex information processing. In our research, we aim to design an Izhikevich-type simple silicon neuron circuit by reproducing the mathematical structure in the original model using analog electronic circuit. It is operated in the subthreshold region of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) for low energy consumption in the Complementary Metal-Oxide-Semiconductor Very Large Scale Integration circuit (CMOS VLSI) technology.

Keywords: Silicon neuron, Izhikevich model, mathematical structure-based method, subthreshold.

I Introduction

Silicon neuron is designed to mimic electrophysiological functions of neurons. Some of silicon neurons are intended to be utilized as an element of artificial spiking neural networks that process complex information in the same manner as the human brain.

There are several approaches to design silicon neurons in the analog electronic circuit. One of them is to reproduce significant neuronal behaviors, the phenomenological method in other words [1]. Another is the conductance-based method which tries to solve the models of ionic conductances in neurons by analog electronic circuits [2].

Recently, Kohno proposed a new approach [3–5], a mathematical-structure-based method, where we re-construct the mathematical structures in the differential equations of neuron models. By applying mathematical techniques, we can design a silicon neuron with simpler circuitry while keeping the neuronal dynamics.

There have been proposed variety types of silicon neurons. Generally, simple silicon neurons can produce only several types of spike patterns whereas complex ones can variety of patterns because the latter reproduces more realistic dynamics in the neurons. Simple silicon neurons are mainly applied to large-scale networks because they need large number of silicon neurons as the element. On the other hand, complex silicon neurons are applied to hybrid systems because they behave very close to the neurons. To construct large-scale spiking neural networks, we need simple silicon neurons that have rich dynamics because recent neuroscientific researches are finding that it is crucial in the information processing in the nerve system.

Izhikevich proposed a simple qualitative neuron model [6, 7], which is able to produce 20 kinds of firing patterns. Though the mathematical structure in the Izhikevich model is very simple, it has nonlinearity, including jump of the state, which makes it possible to produce various firing patterns.

In our research, we aim to design an Izhikevich-type silicon neuron circuit by reconstructing the mathematical structure in the Izhikevich model into a simple circuitry using an analog electronic circuit. We designed a silicon neuron circuit composed of MOSFETs operated under the subthreshold condition for low energy consumption in VLSI. The power supply voltage is 3 3V, Vdd=1 65V and Vss= 1 65V.

II Izhikevich model

The Izhikevich model is 2-variable differential equations that have nonlinearity including jump of state when the membrane potential excesses 30mV :

$$\frac{dv}{dt} = 0\ 04v^2 + 5v \quad 140 + I \tag{1}$$

$$\frac{du}{dt} = a(bv \quad u) \tag{2}$$

$$\text{if} \quad v = 30\text{mV} \quad \text{then} \quad v \leftarrow c \quad u \leftarrow u + d$$

where v is membrane potential and u is an internal variable. This model contains 4 parameters and we can realize various dynamics by setting them up appropriately. Parameter c is the membrane voltage after the jump of state and d is increase amount of u when v is reset. Tunability of dynamics in the Izhikevich model mainly depends on these two parameters.

In the Izhikevich model, parameter b represents the slope of the u-nullcline (Fig. 1(a)), which is difficult to control when this model is implemented in an electrical circuit. To avoid this problem, we control the positional relation between the v- and the u-nullclines instead of b

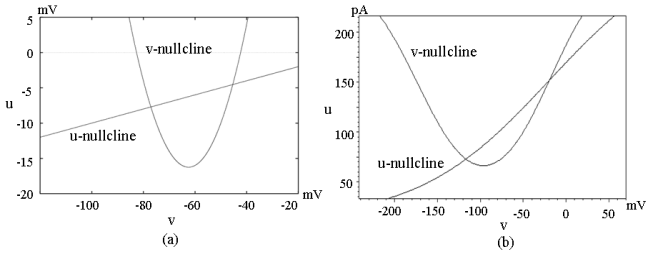

Fig. 1: The phase plane of the Izhikevich model. (a) the original model's phase plane. (b) reconstructed phase plane by utilizing the characteristic curve of differential pair circuits.

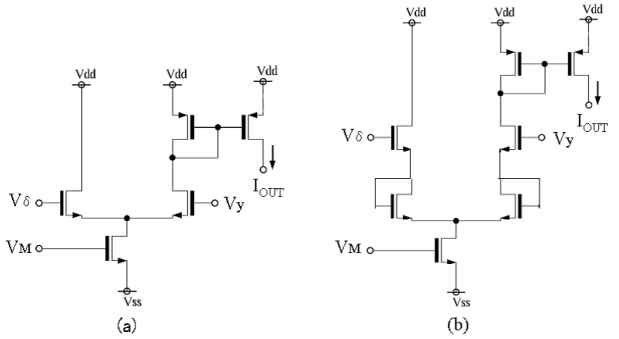

Fig. 2: Schematics of the differential pair circuitries utilized for the composition of the v- and the u-nullclines. M, δ in Eqs. (3) and (4) are applied at the nodes labelled V_{M} and V_{δ}.

This allows us to tune the mathematical structure in our silicon neuron model in the same manner as in the original model. We adopted a new parameter I_{bias}, a bias current into the membrane potential, which is responsible to the positional relation.

III Mathematical method

We applied the mathematical design method proposed by Kohno [3–5] to design an Izhikevich-type silicon neuron model. In this method, we reproduce the mathematical structures in differential equations of neuronal models using output characteristic curves of simple analog electronic circuitries. One of the advantages in this method is that we do not need to exactly copy the equations in the original model. The geometrical features of the nullclines and their positional relationship are reproduced, which allows us to copy the dynamics in the original model by a simple circuitry.

We utilize the sigmoidal curves that are output characteristics of differential pair circuitries to reproduce the geometrical features of the nullclines in the Izhikevich model. The characteristic curves of these differential pair circuits Fig. 2 (a) and (b) are represented in Eqs. (3) and (4), respectively.

$$I_{\mathrm{OUT}} = M\frac{1}{1+exp(\ \ \kappa(y\ \ \delta)\ \ U_{\mathrm{T}})} \tag{3}$$

$$I_{\mathrm{OUT}} = M\frac{1}{1+exp(\ \ \kappa(y\ \ \ \delta)\ \ 2U_{\mathrm{T}})} \tag{4}$$

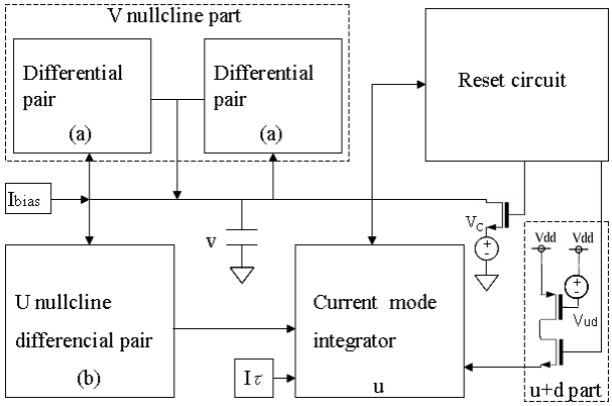

Fig. 3: Brief overview of designated circuit

where κ represents the capacitive coupling ratio and U_{T} is the thermal voltage.

Utilizing these sigmoidal curves, we are able to reconstruct the topological relationships of the Izhikevich model's nullclines (Fig. 1(b)). The v-nullcline in our silicon neuron model is produced by connecting a couple of symmetrical sigmoidal curves. The u-nullcline in the Izhikevich model is linear, which is substituted by a sigmoidal curve.

The v-nullcline of our silicon neuron model is produced by the differential pair circuit shown in Fig. 2(a), and the u-nullcline is by the circuit in Fig. 2(b)

IV Designed circuit

An overviewed diagram of our silicon neuron circuit is shown in Fig. 3. Our circuit consists of the v-nullcline, the u-nullcline, a current-mode integrator, reset circuit, and the u+d module.

1. Current-mode integrator

In our silicon neuron circuit, variable u is represented by an amount of a current. We utilized current-mode integrator to integrate u, which corresponds to the differential equation (2). Figure 4 shows the current-mode integrator circuit designed to operate in the subthreshold region.

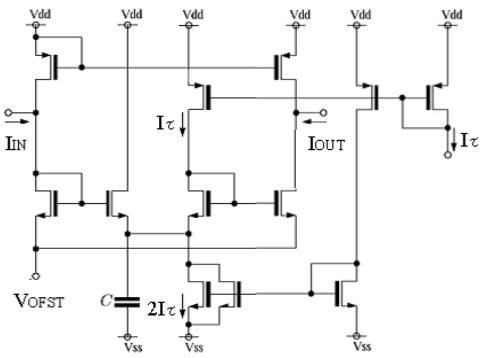

Fig. 4: The schematic of the current-mode integrator. The time constant of Eq. (5) depends on the capacitance and the bias current I_{τ}. We can tune the time constant by tuning I_{τ} externally. V_{OFST} is a bias voltage.

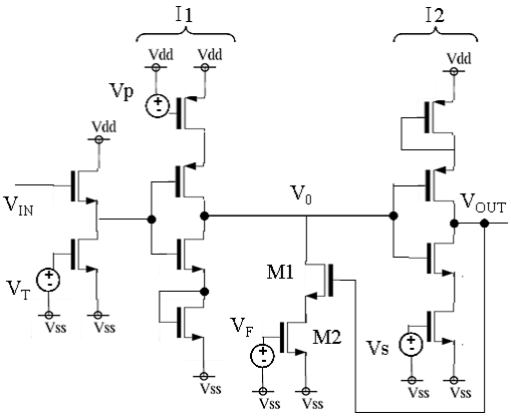

Fig. 5: The schematic of reset circuit. V_T, V_P, V_F and V_S are bias voltages. V_T, V_P and V_F are applied to switch output voltage V_{OUT} high when the input voltage excesses 30mV. M1 and M2 give a positive feedback voltage to inverter I2.

This circuit integrates the input current I_{IN} as follows:

$$\frac{dI_{OUT}}{dt} = \frac{I_\tau}{CU_T}(I_{IN} \quad I_{OUT}) \tag{5}$$

where I_{OUT} and C are the output current and the capacitance in the circuit, respectively. The time constant of the integrator corresponds to the parameter a in the model, which is decided by I_τ. In this circuit, current I_{OUT} is dependent on the voltage of the capacitor. We use this property of the current-mode integrator in the u+d module.

2. reset circuit

In the Izhikevich model, when the membrane potential excesses 30mV, v jumps to potential c and u increases by d. To realize an Izhikevich-type silicon neuron circuit, we have to equip this kind of discontinuity. The circuit for this property is shown in Fig. 5. We refer to it as the reset circuit.

The reset circuit is composed of a source follower, two inverters I1 and I2 and transistor M1 and M2 that give a positive feedback voltage to I2. Node Vo is protected from being shorted to Vss by M2. This function realizes the precipitous response and low power consumption.

3. Parameter control of Izhikevich-type silicon neuron

To realize stable and simple parameter tuning, we focus on I_{bias} and the circuit parameters correspond to a and c in the original model. The v-nullcline is displaced vertically by I_{bias}. We can control the stability of equilibrium points by tuning this parameter (see Fig. 6(a)).

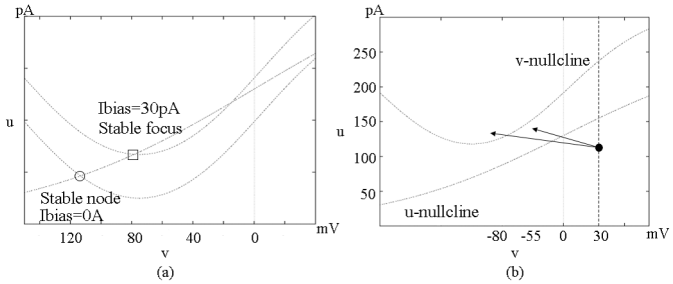

Fig. 6: Parameter control of our Izhikevich-type silicon neuron. (a) The stability of equilibrium points can be controlled by I_{bias}. When I_{bias} is 0A, the equilibrium point is a stable node and when I_{bias} is 30pA, it is a stable focus. (b) Controlling the jumping dynamics by parameter c. When parameter c is 85mV, the state comes inside of the v-nullcline after the first jump, but it is the outside of it when c is 55mV.

4. u+d module

In section IV.1, we mentioned that u depends on the voltage of the capacitance in the current-mode integrator circuit. If we increase this voltage externally, the voltage of u is increased just after the reset circuit performs its function.

The circuit of the u+d module injects current I_P into the capacitor dependent on the reset circuit. Equation (5) is modified as follows if we incorporate the effect of I_P into the integrator circuit.

$$\frac{dI_{OUT}}{dt} = \frac{I_\tau}{CU_T} \; I_{IN} \quad I_{OUT} + I_P exp(\frac{V_C \quad V_{OFF}}{U_T}) \tag{6}$$

where V_C is voltage of the capacitor and V_{OFF} is offset voltage in the current mode integrator. It is not easy to control the exact magnitude of increase in u because the V_C in Eq. (6) changes dynamically while the current-mode integrator is operating. In the Izhikevich model, many firing patterns depend on whether the jumped state is inside the v-nullcline or not. The jumping dynamics is controlled by the parameter c as shown in Fig. 6(b). For example, to produce bursting dynamics, we set c around 55mV where is usually outside of the v-nullcline until the state takes few jumps.

We fix the amount of injection current by setting Vud to 100mV to reduce the number of the parameters to be controlled. By the effect of the leak current in the u+d module, the u-nullcline is displaced to the direction of the u-axis by a few tens of pA in the phase plane.

V Simulation

We simulated our silicon neuron circuit using HSPICE software with the technology library of TSMC .35 μ mixed signal process. Figure 7 shows the results of the simulation. We could successfully produce 17 firing patterns reported in the Izhikevich model by our simplified parameter tuning sheme.

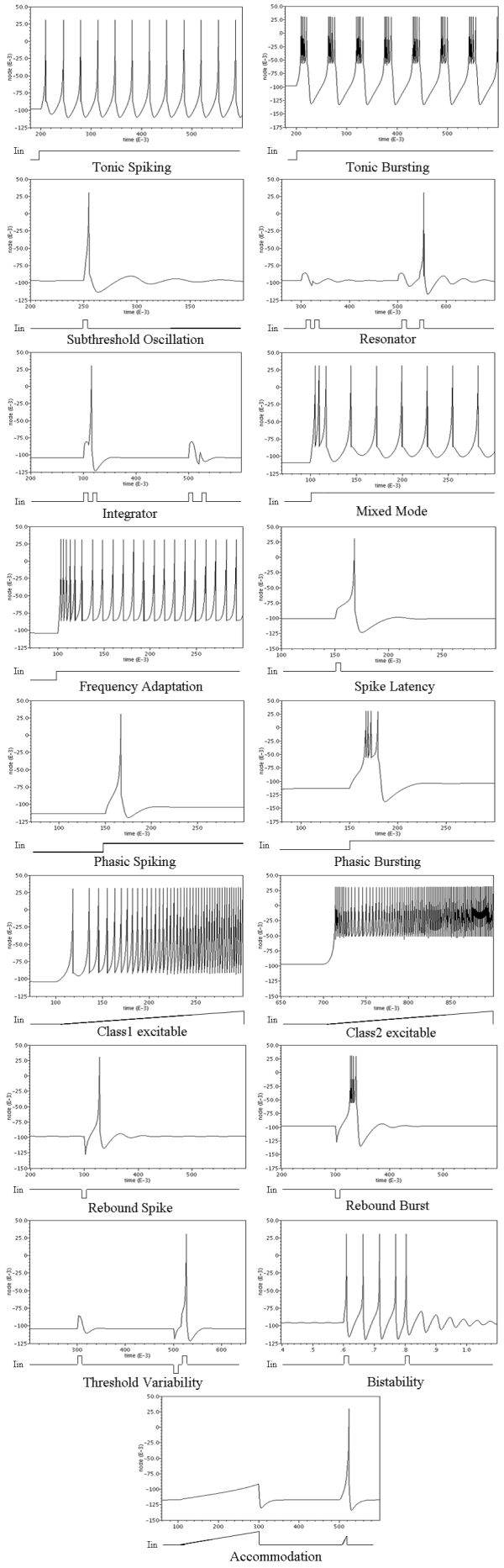

Fig. 7: Produced firing patterns

VI Conclusion

We proposed a simple implementation of an Izhikevich-type silicon neuron. The total number of transistors is 44. In the Izhikevich model, 4 parameters have to be tuned to realize all of the intended firing patterns. By noticing the mathematical structure in the model, we could output these patterns by tuning only 3 parameters. In addition, parameters b can be positive or negative in the original model, but we succeeded to output 17 patterns out of 20 by only positive b. This allows us to reduce the total number of transistors by eliminating extra circuits. In the remaining three patterns, however, parameter a or d is negative, to realize which in the silicon neuron circuit we have to add another circuit blocks. This will be addressed in our future works.

Our circuit is designed to operate with very small power consumption, about 15nW in average.

Acknowledgements

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