Performance Optimization of Forward Converters Based on Genetic Algorithms

Young-Kiu Choi, Dong-Young Woo and Byung-Wook Jung School of Electrical Engineering, Pusan National University Changjeon-dong, Geumjeong-gu, Busan 609-735, Korea (Tel:82-51-510-2371; Fax: 82-51-513-0212) (ykichoi@pusan.ac.kr, blueinside@pusan.ac.kr, wooroogy@pusan.ac.kr)

Abstract: The forward converter is one of power supplies used widely. This paper presents parameter tuning methods to obtain circuit element values for the forward converter to minimize the output voltage variation under load changing environments. The conventional method using the concept of the phase margin is extended to have optimal phase margin that gives slightly improved performance in the output voltage response. For this, the phase margin becomes the tuning parameter that is optimized with the genetic algorithm. Next, the circuit element values are directly considered as the tuning parameters and also optimized using the genetic algorithm to have very improved performance in the output voltage control of the forward converter.

Keywords: forward converter, output voltage control, genetic algorithm

I. Introduction

The forward converter is one of power supplies used widely. It is based on DC/DC converters. DC/DC converters are equipments that transform some DC voltages into required DC voltages. DC/DC converters are usually classified into buck, boost, buckboost and Cúk converters. Forward converters are related to buck converters. Forward converters with rectifier stage on the AC side are used as power supplies that should maintain constant DC output voltages[1-3]. Even though the loads of forward converters often change abruptly, forward converters should keep constant output voltages with some forms of feedback control. A design method proposed by Venable[4,5] using the concept of phase margins has been widely used. It has voltage feedback controllers with error amplifiers composed of OP-Amps, resistors and capacitors. Other design methods using the root locus[6], PI control[7] and robust control[8] were also proposed for the output voltage control of power supplies. These design approaches essentially have some design parameters such as phase margins and gains. The performance of feedback controllers for output voltages is closely related to those design parameters; however, these parameters usually rely on designers' experience. So, we have optimization problems for forward converters with respect to those parameters and the problems may be efficiently solved by genetic algorithms[9].

In this paper, the conventional design method based on the phase margin[5] is optimized with the genetic algorithm for the forward converter; the phase margin is considered as the tuning parameter that is optimized to have some improved output voltage responses. Next, resistances and capacitances of the voltage feedback controllers are directly regarded as the tuning parameters and they are optimized using the genetic algorithm to have very improved response of output voltage in the forward converter.

II. System Configuration of the Forward Converter

Since the output voltages of forward converters are influenced by the change of loads, voltage feedback controls are required to maintain constant output voltages. Fig.1 shows a circuit diagram of the forward converter with the voltage control loop.

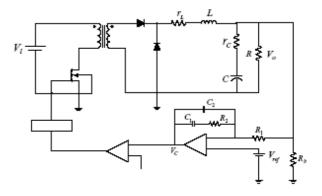


Fig. 1. Forward converter with voltage control loop

Let $G_P(s)$ be a transfer function relating the output voltage $v_O(s)$ to the control voltage $v_C(s)$. Then we have The Thirteenth International Symposium on Artificial Life and Robotics 2008(AROB 13th '08), B-Con Plaza, Beppu, Oita, Japan, January 31-February 2, 2008

$$G_{P}(s) = \frac{V_{i}/V_{P}}{LC} \left[\frac{1 + sr_{C}C}{s^{2}\left(1 + \frac{r_{C}}{R}\right) + s\left(\frac{1}{RC} + \frac{r_{C}}{L} + \frac{(r_{C} + R)r_{L}}{RL}\right) + \frac{(r_{L} + R)}{RLC}} \right]$$
(1)

where V_i is the input source voltage, V_P is the peak voltage of PWM circuits, and R is the load resistance. L is the inductance of the inductor coil, r_L is the resistance of the inductor coil, C is the capacitance of the capacitor, and r_C is the equivalent series resistance of the capacitor.

We should have proper values of circuit elements of R_1 , R_2 , C_1 and C_2 of the error amplifier in Fig. 1 to minimize the variation of the converter output voltage caused by the change of the load resistance R. The conventional procedure to select the proper values of the circuit elements is as follows[5].

- Plot the Bode diagram of G_P(s)
- Select a desired bandwidth ω_{CO} (= ω_S/10 ~ ω_S/5), where ω_S is the switching frequency. Find R₁ and R₂ such that G_P(jω_{CO}) = R₁/R₂.
- iii) Choose a proper phase margin (PM) that should be usually greater than or equal to 45°. Calculate the following equations:

$$\varphi_{CO} = PM - \angle G_P(j\omega_{CO}) - 180^{\circ} \qquad (2)$$

$$K^2 - 2 \tan(\varphi_{CO} + 90^\circ)K - 1 = 0$$
 (3)

iv) Find the zero frequency ω_Z and pole frequency ω_P :

$$\omega_Z = \omega_{CO} / K$$
, $\omega_P = K \omega_{CO}$ (4)

v) Finally, C₁ and C₂ are obtained as follows:

$$C_1 = 1/(R_2 \omega_Z), \quad C_2 = 1/(R_2 \omega_P)$$
 (5)

III. Parameter Tuning Method Using Genetic Algorithms

In the conventional procedure previously stated, the phase margin should be chosen to minimize the variation of the output voltage of the converter caused by the load change; however, the optimum value of the phase margin is not known. In this paper, the phase margin is considered as the tuning parameter and the genetic algorithm is applied to optimize the phase margin to find the values of R_1 , R_2 , C_1 and C_2 of the error amplifier minimizing the output voltage variation. To improve further the circuit performance beyond the conventional procedure based on the phase margin, we have R_1 , R_2 , C_1 and C_2 themselves as the tuning parameters, i.e., the chromosomes of the genetic algorithm. The chromosomes are encoded to be binary forms of 32 bits. The cost function J and the fitness F for the genetic algorithm are defined as below:

$$J = \int_{0}^{T_f} |e(t)| dt \qquad (6)$$

where e(t) is the output error voltage that is the difference between the reference voltage V_{ref} and the output voltage $v_o(t)$. T_f is the final time for evaluation of the cost function.

$$F = \frac{1}{1 + \alpha J}$$
(7)

where α is a weighting factor for the fitness value.

Fig. 2 shows the total flow chart for parameter tuning procedure with the genetic algorithm. PM denotes the phase margin.

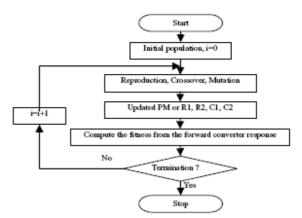


Fig. 2. Flow chart of the parameter tuning algorithm

IV. Simulation Results and Discussion

Let the forward converter in Fig. 1 have the following values:

$$\begin{split} &V_t = 8V \ , V_{ref} = 5V \ , L = 5\mu H \ , r_L = 20m\Omega \ , C = 2000\mu F \ , \\ &r_c = 10m\Omega \ , V_p = 3V \ , \omega_{co} = 6.66\pi \times 10^4 [rad/s] \ . \end{split}$$

The load resistance R is set to be 0.2Ω in the time interval $0 \sim 0.6ms$, is changed to be 0.1Ω in the time interval $0.6ms \sim 1ms$, and is set to be 0.2Ω again in the time interval $0.6ms \sim 1ms$. T_f in eq.(6) is 1.5ms and α in eq.(7) is 2×10^5 .

Given the phase margin 50° that is arbitrarily chosen, the conventional procedure previously stated for the forward converter generates the following element values: $R_1 = 20k\Omega$, $R_2 = 800.84k\Omega$, $C_1 = 23.184 pF$, and $C_2 = 1.5332 pF$.

The cost function J is 3.8582×10^{-6} and the output voltage of the forward converter is shown in Fig. 3.

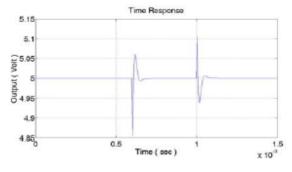


Fig. 3. Output voltage of the forward converter with the phase margin 50°

Next, the genetic algorithm is applied to optimize the phase margin. The phase margin is encoded to be 20-bit binary chromosomes, the population size is 100, the crossover rate is 0.75, the mutation rate is 0.008, and the number of generations is 50. The load resistance R is changed in the same way as before. As a result, the cost function J is 3.2361×10^{-6} and the optimized phase margin is 65.41° . Fig. 4 shows the output voltage response of the forward converter that is slightly improved compared to that in the case of the phase margin 50° .

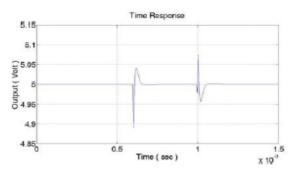


Fig. 4. Output voltage of the forward converter with the phase margin 65.41

The circuit element values are also a little bit changed: $R_1 = 20k\Omega$, $R_2 = 800.84k\Omega$, $C_1 = 50.623pF$, $C_2 = 0.70217 pF$.

To improve the output voltage response further, R_1 , R_2 , C_1 and C_2 are directly regarded as the tuning parameters and encoded in the form of 32-bit binary chromosomes, and then the genetic algorithm is applied to tune the parameters. The population size is 100, the crossover rate is 0.75, the mutation rate is 0.008, and the number of generations is 30. The load resistance R is changed in the same way as before. The cost function J is so much decreased to be 5.8164×10^{-7} and the circuit parameters are $R_1 = 1k\Omega$, $R_2 = 198.82k\Omega$, $C_1 = 117.65 \, pF$ and $C_2 = 0.49412 \, pF$. Fig. 5 shows the output voltage response of the forward converter that seems very improved when compared to that of the phase margin

65.41° in the sense of the magnitude and duration of the transient response: the magnitude decreased 65.8% and the duration also decreased 30.8%.

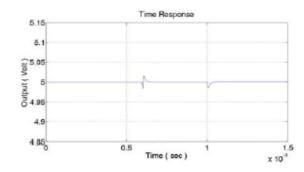


Fig. 5. Output voltage of the forward converter in the final case

V. Conclusions

The forward converter is one of power supplies with precise voltage regulation. This paper presents a parameter tuning method using the genetic algorithm to obtain circuit element values to minimize the output voltage variation under various load conditions. First, an optimal phase margin for the conventional procedure has been obtained using the genetic algorithm; however, it ensures only a little bit improvement over the phase margin 50° that was arbitrarily chosen. Second, two resistances and two capacitances of the error amplifier are considered as the tuning parameters, and the genetic algorithm is also applied. The optimal parameters give us very improved control performances for the output voltage of the forward converter.

REFERENCES

- Mohan N, Undeland TM, and Robbins WP (2003), Power Electronics. 3rd edn. John Wiley & Sons, Inc.
- [2] Chen YM, Liu YC, and Lin SH (2006), Double-input PWM DC/DC converter for high-/low-voltage sources. IEEE Trans. on Industrial Electronics 53(5): 1538-1545
- [3] Wei S and Lehman B (2007), Current-fed dual-bridge DC-DC converter. IEEE Trans. on Power Electronics 22(2): 461-469
- [4] Venable D (1983), The K factor: a new mathematical tool for stability analysis and synthesis. Proceedings Powercon 10
- [5] Hart DW (1996), Introduction to Power Electronics, Prentice-Hall
- [6] Guo L, Hung JY, and Nelms RM (2003), Digital controller design for forward and boost converters using root locus. Proceedings IEEE IECON: 1864-1869
- [7] Guo H, Shiroishi Y, and Ichinokura O (2003), Digital PI controller for high frequency switching DC/DC converters based on FPGA. Proceedings IEEE INTELEC: 536-541
- [8] Higuchi K, Nakano K, Kajikawa T, Takegami E, Tomioka S, and Watanabe K (2004), Robust control of DC-DC converter by high-order approximate 2-degree-of-freedom digital controller. Proceedings IEEE IES: 1839-1844

The Thirteenth International Symposium on Artificial Life and Robotics 2008(AROB 13th '08), B-Con Plaza, Beppu, Oita, Japan, January 31-February 2, 2008

> [9] Michalewicz Z (1996), Genetic Algorithms + Data Structures – Evolution Programs. 3rd edn. Springer-Verlag, Berlin Heidelberg, New York