MOSFET Implementation of Class I* Neurons Coupled by Gap Junctions

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Abstract

This paper proposes a class I* neuron circuit coupled by gap junctions (GJs) consisting of enhancement-type MOSFETs. Some neurons that belong to a subclass of class I, when coupled by GJs, exhibit extensive spatio-temporal chaos in some parameter regions. This subclass is called class I* and characterized by a phase plane structure called a narrow channel. In the proposed circuit, one can metamorphose the model continuously - class I*, class I without a narrow channel, and even to class II - by changing the value of the resistance. The circuitry is compatible with standard CMOS semiconductor processes. Hence it can be implemented in an analog very-large-scale integrated circuit (aVLSI) and the construction of a relatively large network is possible. We show PSPICE simulation results for a circuit implementeted with discrete elements. A GJ-coupled network consisting of twenty such neurons is shown to reveal itinerant dynamics similar to class I* GJ-couple systems.

1 Introduction

Neuromorphic hardware has been studied extensively, and various circuitries have been proposed to emulate biological neurons [1]. Some studies implement conductance-based models [3] such as the Hodgkin-Huxley (HH) model and others implement phenomenological models [4] such as the integrate-and-fire (I&F) model. The I&F neuron is very simple and more popular for studies of large network dynamics, but biological neurons have more complex electrical dynamics. On the other hand, the HH model describes in detail the electrical dynamics of biological neurons. It is difficult to analyze mathematically because this model includes four-dimensional nonlinear differential equations.

As Hodgkin pointed out, there are two classes of neurons: class I and class II [5]. When a strong enough sustained current is applied, neurons fire repetitively. The firing frequency of class I neurons at the onset is asymptotically zero, whereas that of class II neurons is nonzero. It is well known that saddle-node bifurcation produces class I excitability, and the subcritical Hopf bifurcation class II. These bifurcations can be generated in two-dimensional systems. Thus, we adopt two-dimensional reduction models of neurons so that the temporal evolution of the variables can be visualized in the phase plane.

Recent physiological data indicate the massive presence of gap junctions (GJs) among the interneurons in the neocortex [6] [7]. They raise a serious question about the role of interneurons for neural coding and the dynamics of system levels for inhibitory neurons electronically coupled by GJs. Fujii et al. claimed that some neurons that belong to a subclass of class I, when coupled by GJs, can exhibit extensive spatio-temporal chaos in some parameter regions [8]. This subclass is characterized by a phase plane structure called a narrow channel. They named these neurons class I*. They show perfectly regular firings when isolated, so this chaotic behavior is an emergent property of coupled systems.

In this paper, we propose a class I* silicon neuron circuit, that has a simple phase plane structure. In the following section we briefly summarize the class I* neuron models. In Section 3 we describe the characteristics of the silicon neuron circuitry and PSPICE simulation results for a circuitry implemented with discrete elements. Finally in Section 4 we make concluding remarks.

2 Class I* Neuron Models

The two-dimensional reduction models of a single cell are written as [10]

$$\begin{cases} \tau_V \dfrac{dV}{dt} = F(V,R) + I \\ \tau_R \dfrac{dR}{dt} = G(V,R) \end{cases}, \tag{1}$$

where V represents the membrane potential, R is the conductance parameter of the ion channels, and I is the stimulus current. In two-dimensional reduction models, dynamic behavior can be characterized in the two nullclines corresponding to the two variables. In many case,

the class I neurons have U-shaped R-nullclines, while the class II neurons have inclined I-shaped R-nullclines. Most neurons have inverted-N-shaped V-nullclines.

The essential nonlinearity of class I* is characterized by (1) the presense of a narrow channel, (2) the presence of an unstable spiral, and (3) the presence of orbits (with positive measure) reentering into the channel. It is not difficult to construct class I* models. The neuron models with inverted-N-shaped V-nullclines and U-shaped R-nullclines can be turned into class I* by adjusting the parameters.

3 The Silicon Neuron

In this section, we describe the characteristics of the proposed circuits and present PSPICE simulation results with discrete elements (NEC $\mu PA602$ and $\mu PA603$). These two devices are a complementary pair. The supply voltages are $V_{DD} = 5.0$ V and $V_{SS} = -5.0$ V.

3.1 Circuit Operation and Characteristics

Tne neuron circuit mainly consists of three blocks (see Fig. 1): inverted-N-shaped nonlinear resistance, U-shaped nonlinear resistance, and V-I converter.

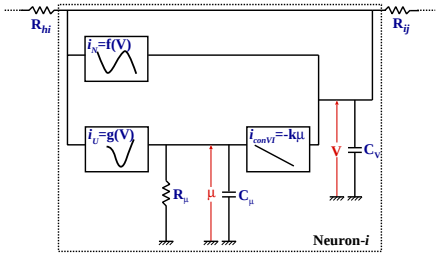

Figure 1: Block diagram of class I* neuron circuits.

The circuit equations of this silicon neuron are

$$\begin{cases} C_V \dfrac{dV}{dt} = f(V) - k\mu \\ C_\mu \dfrac{d\mu}{dt} = g(V) - \dfrac{\mu}{R_\mu} \end{cases}, \qquad (2)$$

where C_V is the membrane capacitance, V represents the membrane potential, k is the ratio of V-I converter, μ is the channel conductance variables, C_μ represents the time constant of μ, R_μ is the constant resistance, $f(V)$ is the inverted-N-shaped-nonlinear resistance, and $g(V)$ is the U-shaped nonlinear resistance.

Fig. 2 shows a schematic of the V-I converter. The source-follower M31-M32 produces $V'_{IN} \simeq V_{IN} + V_{DD} - V_{conVI}$, where V_{IN} is the input voltage and V_{conVI} is a constant bias voltage. The feedback M33-M34 has the effect of suppressing the nonlinearity of the input/output (IO) characteristics. Hence the output current of this circuit may be expressed as $I_{conVI} \simeq -kV'_{IN} + \Delta I$, where k is the ratio of the V-I converter. This ratio can be altered by R_{conVI}.

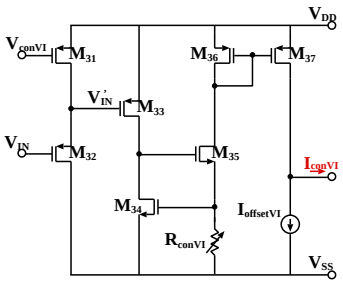

Figure 2: Schematic of the V-I converter.

Fig. 3 shows the IO characteristics of the V-I converter. This circuit is very simple and has good linearity.

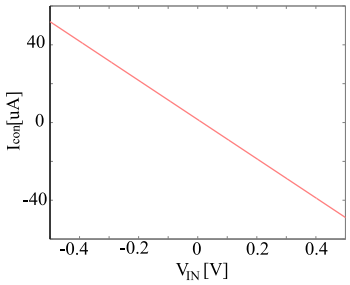

Figure 3: IO Characteristics of V-I converter. V_{conVI} =2.8 V, R_{conVI} =10 kΩ, $I_{offsetVI}$ =0.24 mA.

The inverted-N-shaped nonlinear resistance is schematically shown in Fig. 4. This circuit consists of a differential pair M1-M2 and a V-I converter M5-M9. The output current of this circuit may be expressed as $I_N = I_{diffN} + I_{conN}$, where I_{diffN} is the output current of the differential pair and I_{conN} is the output current of the V-I converter respectively.

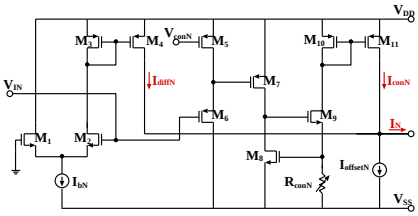

Figure 4: Schematic of inverted-N-shaped circuit.

Fig. 5 shows the I-V characteristics of this circuit. These characteristics represent the V-nullcline of the silicon neuron.

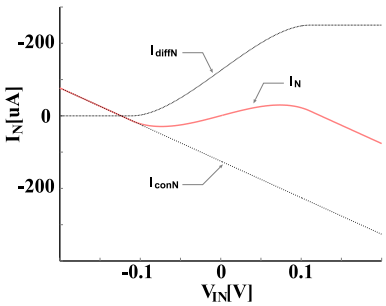

Figure 5: I-V characteristics of inverted-N-shaped nonlinear resistance. I_{bN} =0.25 mA, V_{conN} =2.8 V, R_{conN} =1 kΩ, $I_{offsetN}$ =2.54 mA.

A schematic of the U-shaped nonlinear resistance is shown in Fig. 6. This circuit consists of an improved anti-bump circuit M12-M19 and the V-I converter M22-M26. The differential pair M12-M15 is used to shift the input voltage V_{IN} by a constant voltage V_{bump}. The original anti-bump circuit [2] takes two input voltages, V_1 and V_2, and generates three output currents. The two outside currents, I_1 and I_2, are a measure of the dissimilarity betweeen the two inputs; the center current I_{mid} is the measure of the similarity. Hence this circuit has Gaussian-like I-V characteristics. In the proposed circuit, V_2 is connected to GND, and the amplitude of V_1 can be altered by the resistance R_{bump} to adjust the left slope of the Gaussian curve. The output current of this circuit may be expressed as $I_U = I_{bump} - I_{conU}$, where I_{bump} is the output current of the improved anti-bump circuit and I_{conU} is the output current of the V-I converter. The I-V characteristics of this circuit represent the μ-nullcline of the silicon neuron.

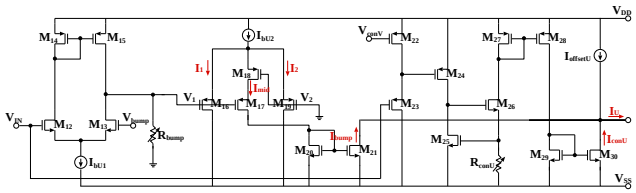

Figure 6: Schematic of U-shaped nonlinear resistance.

3.2 Behavior of The Single Neuron

The phase plane structure of the silicon neuron is shown in Fig. 7. By changing the value of R_{bump}, we can metamorpose the model continuously: class I*, class I without a narrow channel, and class II.

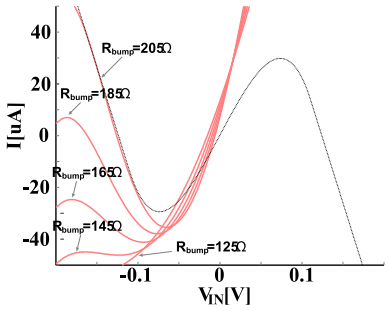

Figure 7: Nullcline of the proposed silicon neuron. The dashed line is μ-nullcline and the solid line is V-nullcline. I_{bN} =0.25 mA, V_{conN} =2.8 V, R_{conN} =1 kΩ, $I_{offsetN}$ =2.54 mA, I_{bU1} =0.9 mA, V_{bump} =5 mV, I_{bU2} =4 mA, V_{conU} =2.8 V, R_{conU} =4 kΩ and $I_{offsetU}$ =1.35 mA.

Fig. 8 shows the membrane potential V of the silicon neuron for the phase plane structure in Fig. 7. The single silicon neuron shows perfectly regular firings.

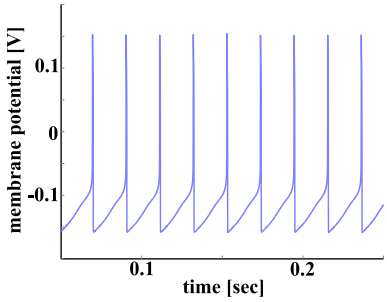

Figure 8: Time course of the membrane potential of the proposed silicon neuron. C_V =10 nF, C_μ =100 nF, R_μ =10 kΩ, k ≃0.1 mS and R_{bump} =205 Ω

3.3 Itinerant Dynamics in Class I* GJ-Coupled Systems

The currents induced by GJs are [9]

$$\begin{aligned} J_i &= \frac{1}{R_{GJ}} \sum_{nb_i} (V_{nb_i} - V_i) \\ &= g_{GJ} \sum_{nb_i} (V_{nb_i} - V_i), (nb_i \in coupledneigborcell), \end{aligned} \tag{3}$$

where g_{GJ} is a coupling constant, which is assumed to be identical for all connections in this simulation. The neurons at the boundaries connect only to the inner neurons.

Fig. 9 shows the time series of the GJ-coupled network that consists of twenty of the proposed circuits.

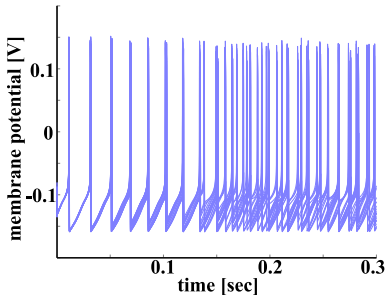

Figure 9: Time series of the GJ-coupled network consisting of twenty of the silicon neurons. R_{GJ} =10 kΩ.

At time t=0, there is a slight variation in the charges of the capacitors (C_V, C_μ) of the neurons. This system has been shown to exhibit chaotic dynamics as time elapses. Note that each neuron shows perfectly regular firings when isolated. Hence this chaotic behavior is an emergent property of coupled systems.

4 Concluding Remarks

We have proposed a class I* silicon neuron circuitry with a simple phase plane structure. We combined inverted-N-shaped and U-shaped nullclines to reproduce the narrow channel structure. Differential pair circuitries, bump circuitries, and linear resistances were employed to implement these nullclines. Their I-V characteristics can be easily altered by external voltages and resistances. The varieties of I-V characteristics allow the proposed circuit to behave as a class I*, class I, or class II neuron. We have also shown PSPICE simulation results for a circuit implemented with discrete elements. A GJ-coupled network consisting of twenty neurons was shown to generate itinerant dynamics similar to class I* GJ-coupled systems in the work of Fujii et al. Moreover, this circuitry is compatible with standard CMOS semiconductor processes. Hence it can be implemented in an analog very-large-scale integrated circuit (aVLSI) and the construction of relatively large networks is possible as well.

Acknowledgements

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References

[1] M. Mahowald and R. Douglas, “A Silicon Neuron”, *Nature*, Vol. 354, pp. 515-518, 19/26 Dec. 1991.

[2] T. Delbruck, “Bump Circuits for computing similarity and dissimilarity of analog voltages”, *IJCNN*, pp. I-472-479, 1991.

[3] Simoni MF., Cymbalyuk GS., Sorensen ME., Calabrese RL. and DeWeerth SP., “A Multiconductance Silicon Neuron With Biologically Matched Dynamics”, *IEEE Trans Biomed Eng.*, Vol. 51(2) pp. 342-54, Feb. 2004.

[4] G. Indiveri, “A low-power adaptive integrate-andfire neuron circuit”,*In ISCAS 2003. The 2003 IEEE International Symposium on Circuits and Systems, 2003. IEEE* , 2003.

[5] Hodgkin A.L., “The local electric changes associated with repetitive action in a non-medullated axon”, *J. Physiology*, Vol. 107, pp. 165-181, 1948.

[6] Galarreta M. and Hestrin S., “A network of fast-spiking cells in the neocortex connected by electrical synapses”, *Nature*, Vol. 402, pp. 72-75, 1999.

[7] Gibson JR, Beierlein M and Connors BW, “Two networks of electrically coupled inhibitory neurons in neocortex”, *Nature*, Vol. 402, pp. 75-79, 1999.

[8] H. Fujii and I. Tsuda, “Itinerant dynamics of class I* neurons coupled by gap junctions”, *COMPUTATIONAL NEUROSCIENCE: CORTICAL DYNAMICS LECTURE NOTES IN COMPUTER SCIENCE*, Vol. 3146, pp. 140-160, 2004.

[9] N. Schweighofer, K. Doya and M. Kawato, “Electrophysiological Properties of Inferior Olieve Neurons: A Compartment model”, *J. Neurophysiol.*, Vol. 82 pp. 804-817, 1999.

[10] Rinzel J., “Excitation dynamics: insights from simplified membrane models”, *Fed. Proc.*, Vol. 44, pp. 2944-2946, 1985.