A Multistage Heuristic Tuning Algorithm for an Analog Silicon Neuron Circuit

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Abstract
This research looks at an ultra-low power subthreshold-operated silicon neuron circuit designed with qualitative neuronal modeling. One technical challenge to future implementation of such circuits is parameter tuning—a problem stemming from temperature sensitivity of subthreshold-operated MOSFETs and the uniqueness of individual circuits in a neuronal network due to transistor variation. This research proposes a fully automated parameter tuning algorithm that combines two heuristic approaches to search for appropriate circuit parameters over a range of temperatures. The algorithm can tune the circuit to behave as a Class I or Class II neuron.

Keywords: neuromorphic engineering, analog VLSI, silicon neurons

1. Introduction
Analog silicon neurons, electronic circuits that mimic the electrophysiological characteristics of neuronal cells, may in the future be used as fundamental building blocks of neuromorphic technologies like brain-mimetic computers. These circuits operate in continuous time, consume low power, and are expected to be implemented in massively parallel networks that are fundamentally different from digital transistor logic circuits1. The circuit used in this research is an ultra-low power analog silicon neuron designed with the techniques of qualitative modeling—an approach which seeks to reduce the complexity of ionic conductance models by describing the same dynamics with fewer variables2. Such a model allows for replication of a wide variety of spiking dynamics in neuronal cells, including Class I and Class II in Hodgkin’s classification3, with a less complex low power circuit. Power consumption is further reduced by operating the circuit’s metal-oxide-semiconductor field-effect transistors (MOSFETs) in their subthreshold regime4.

The large number of circuit parameter voltages, the temperature sensitivity of subthreshold-operated MOSFETs, and the problem of transistor variation among circuits of equivalent design means that effective parameter tuning to achieve consistent neuron-like dynamics is a significant challenge. A parameter tuning algorithm that addresses these issues will be necessary for future implementation of these circuits in large scale networks.

This research is inspired by positive results in [5] in which the Differential Evolution (DE) algorithm was used to tune the parameter voltages of a conductance-based silicon neuron circuit. The DE algorithm is an evolutionary algorithm which begins with random solution vectors, in this case vectors of circuit parameter voltages, evaluates their performance with a cost function, and passes on elements of vectors with good performance to the next generation6.

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In [7], we presented a script which pairs the Spectre circuit simulator with optimization algorithms to automatically search for optimum circuit parameter voltages over a range of temperatures. Two heuristic approaches were used to improve upon a previous trial-and-error based tuning method. In this paper, we present a multistage tuning algorithm which combines those two heuristic methods with consideration given to their merits and drawbacks, and adds an additional pretuning stage to make the algorithm completely automated. Our new algorithm eliminates the need for trial-and-error, only requires input of benchmark characteristics, and can tune the circuit to behave as a Class I or Class II neuron over a range of temperatures.

2. Circuit Description

The silicon neuron circuit is divided into a v-block and an n-block which each integrate the currents from transconductance circuit components over a capacitor. Variables \( v \) and \( n \) represent membrane potential and abstracted ionic activity and are coded by subtracting the voltage over their respective capacitors from \( V_{dd} \). The system equations are as follows:

\[
\frac{dv}{dt} = f(v) - g(v) + I_v + I_{stim}
\]

The current-voltage relationships for \( f(v), g(v) (x=v,n) \), and \( r(n) \) are sigmoidal curves. A detailed description of these circuits is given in [2]. \( I_{vdc} (x=v,n) \) are transconductance amplifiers used as constant current sources and \( I_{stim} \) is an externally applied stimulus current. Transconductance amplifiers \( TAV \) and \( TAN \) use a voltage clamp method to draw the nullclines—curves on which the system equations equal zero—which are used to describe the dynamics of the silicon neuron. All transistors in the silicon neuron circuit are operated in their subthreshold regime, yielding desirable exponential current-voltage characteristics and power consumption as low as 3 nW.

3. Multistage Parameter Tuning Algorithm

Our algorithm requires the user to input the benchmark circuit characteristics: the nullcline structure, circuit behavior detailed in Sec. 3.3, and current-voltage curves of the \( I_{vdc} \) and \( r(n) \) circuits \( (x=v,n) \) at 27°C. The user then sets the target temperature that circuit parameter voltages are generated for.

Circuit simulations were conducted in the Cadence software environment with the Spectre circuit simulator on two X5570 processors (2.9 GHz, 8 threads).

3.1. Stage I: Pretuning

As listed in Table 1, parameter voltages \( I_{vdc} \) and \( r(n) \) scale the current-voltage characteristics of the \( I_{vdc} \) and \( r(n) \) circuits \( (x=v,n) \). The first stage of the algorithm uses Differential Evolution to find the optimum value of these parameters at the target temperature. The cost function is the mean absolute difference of the current-voltage curve resulting from a given parameter to the

![Image of silicon neuron circuit](image-url)
current-voltage curve of the circuit with benchmark settings at 27°C.

\[ f(x) = \frac{1}{k} \sum_{i=1}^{k} |I(x) - b_i| \] (3)

\( x \) is the parameter value for a given simulation, \( I(x) \) represents each point on the current-voltage curve yielded by a given parameter value, \( b_i \) represents each point on the benchmark curve, and \( v = 0 \) V when \( k = 1 \) and \( v = 1 \) V when \( k = 101 \). The DE algorithm is used once for each of these three circuits, requiring about 1.5 minutes and 130 iterations.

3.2. Stage II: Nullcline tuning

The second stage of the algorithm uses the DE algorithm to tune the nullclines to match the benchmark nullclines at 27°C in the range of 300–450 mV. Spectre simulations of the silicon neuron circuit’s nullcline mode are run with the input being a vector of circuit parameters \( g_{\text{Vn}}, f_{\text{Vb}}, \) and \( l_{\text{x-Vn}}(x=y,n) \). The functions of these parameters are listed in Table 1. \( f_{\text{Vb}}, g_{\text{Vn}}, \) and the scaling factors for the \( l_{\text{in}} \) circuits from the pretuning stage and \( f_{\text{Vb}} \) are kept constant. The \( r(n) \) circuit is set to zero in the nullcline mode and is not directly evaluated.

The cost function is the magnitude of the vector of the mean absolute differences of the \( v \) and \( n \) nullclines from their respective benchmark nullclines.

\[ g(x) = \sqrt{\left( \frac{1}{k} \sum_{i=1}^{k} |v_i(x) - b_i| \right)^2 + \left( \frac{1}{k} \sum_{i=1}^{k} |n_i(x) - c_i| \right)^2} \] (4)

\( v_i(x) \) and \( n_i(x) \) represent the points on the output \( v \) and \( n \) nullcline curves for parameter settings \( x \), \( b_i \) and \( c_i \) represent the points on the benchmark \( v \) and \( n \) nullclines at 27°C, and \( v = 300 \) V when \( k = 1 \) and \( v = 450 \) V when \( k = 151 \). Differential Evolution for this stage of the algorithm typically requires 7 thousand nullcline mode simulations and 4 hours of calculation time.

As reported in [7], the DE algorithm accurately replicated the benchmark nullclines at a variety of temperatures, but did not yield accurate transient behavior, suggesting the need for an additional tuning stage.

3.3. Stage III: Tuning transient behavior

The final stage of the algorithm uses \( m_{\text{Vm}} \) from Stage I and \( g_{\text{Vm}}, f_{\text{Vb}}, \) and \( l_{\text{x-Vb}}(x=y,n) \) from Stage II as the center of a 5 × 5 search space by adding +/- 0.5 and +/- 1 mV to each of these five parameter values. A brute force approach is then used to evaluate each of the \( 5^5 = 3125 \) combinations of parameters in this search space by running transient simulations of the circuit. For Class I mode, the simulation first approximates the silicon neuron’s threshold current to generate a neuronal spike by sending successively stronger 500 \( \mu \)s pulse stimuli in intervals of 8.9 \( \mu \)A, 5% of the benchmark threshold current of 178.5 \( \mu \)A. The time \( v \) rises above 450 mV is recorded. This value roughly corresponds to the threshold current. The circuit is then subjected to 5 and 10 \( \mu \)A sustained stimuli and the spiking frequency is evaluated using data from an 800 ms time period.

The cost function evaluates each parameter set by calculating the magnitude of the difference vector between these three simulated circuit behaviors \( j(x) \) and their benchmark values \( b \), a vector calculated from simulation results with a parameter set which yields typical Class I behavior.

\[ j(x) = \begin{bmatrix} \text{threshold index} \\ \text{5 pA stimulus response} \\ \text{10 pA stimulus response} \end{bmatrix}, \quad b = \begin{bmatrix} 1.21 \\ 15.87 \\ 37.18 \end{bmatrix} 
\]

\[ h(x) = ||j(x) - b|| \] (5)

Class II neurons do not show a clear threshold to generate a neuronal spike and instead are characterized by the sudden onset of periodic spiking when subject to an adequately strong sustained stimulus. The cost function in Class II mode evaluates a vector of the circuit’s frequency response to 5, 7.5, 10, and 12.5 \( \mu \)A sustained stimuli. \( b \) again was calculated from simulation results with a parameter set which results in typical Class II behavior.

\[ j(x) = \begin{bmatrix} \text{5 pA stimulus response} \\ \text{7.5 pA stimulus response} \\ \text{10 pA stimulus response} \\ \text{12.5 pA stimulus response} \end{bmatrix}, \quad b = \begin{bmatrix} 0 \\ 22.08 \\ 30.21 \\ 35.3 \end{bmatrix} \] (6)

Stage III concludes with a polishing step which interpolates the optimum parameter set between the
members of the original search space. This stage requires about 4 hours of calculation time to run all the transient circuit simulations. Increasing the search space exponentially increases calculation time, thus illustrating the need for nullcline tuning in Stage II.

4. Results

The algorithm was run in Class I and Class II modes for 2° to 47°C in 5° steps and the results are listed in Table 2. In Class I mode, the circuit displayed behavior closest to the benchmark in the range of 12° to 42°C. 2°, 7°, and 47° did not yield neuron-like behavior. The threshold current descended from 241 to 123 pA as temperature increased.

In Class II mode, transient behavior nearly identical to the benchmark was observable for 32° and 37°C. At 7°, 12°, and 22°C the 10 pA and 12.5 pA sustained stimuli induced spiking at a similar frequency to the benchmark, but the 7.5 pA response decayed after a few iterations. A simplified version of the algorithm which does not contain the Iax-Vb tuning step in Stage I yielded behavior nearly identical to the benchmark at 22°, suggesting that slight modifications to the algorithm may improve the decaying problem for 7–22°C.

5. Discussion

The multistage heuristic tuning algorithm considers the merits and drawbacks of the DE algorithm-based nullcline tuning and brute force transient tuning approaches as noted in [7] and combines them into a hybrid approach which in simulation can effectively tune the silicon neuron circuit to behave as a Class I or Class II neuron over a range of temperatures. The next step will be to implement a version of this algorithm with the actual silicon neuron circuit using LabVIEW or Python.

This algorithm could also be effective in dealing with issues of transistor variation in a network of silicon neurons, since it can find unique parameter sets which may yield similar nullcline structure among individual members of a network. Future silicon neuron circuits may be designed with on-chip feedback mechanisms which automatically adjust parameter voltages based on the results of a tuning algorithm.

Acknowledgements

This study was supported by JST PRESTO and CREST, and VDEC, the University of Tokyo in collaboration with Cadence Design Systems, Inc.

References


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