High CMRR and Wideband Current Feedback Instrumentation Amplifier Using Current Conveyors

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Abstract

This paper presents a high CMRR and wideband current feedback Instrumentation Amplifier (IA). The proposed IA architecture consists of Fully Balanced Differential Difference Amplifier (FBDDA) and Differential Difference Amplifier (DDA) based on 2nd generation current conveyor (CCII) with a buffer. From the simulation results evaluated by HSPICE, the proposed IA exhibits average CMRR was 109.3 dB higher than the conventional one. Furthermore, the proposed IA has higher closed-loop gain over a larger bandwidth than corresponding voltage feedback.

Keywords: Instrumentation Amplifier, CMRR, Current Conveyor, Differential Difference Amplifier, Current Feedback

1. Introduction

Instrumentation Amplifier (IA) with high CMRR, high input impedance, and configurable differential gain characteristics is used in many application areas, such as medical instrumentation, the read-out circuit of biosensors, signal processing, and data acquisition [1].

Fig.1 shows the conventional IA, which consists of 3 operational amplifiers and 7 resistors. Each resistors require the condition of $R_1 = R_2$, $R_3 = R_4$, $R_5 = R_6$. In this case, the output voltage is described by Eq. (1).

$$V_{out} = \frac{R_5}{R_3}\left(1 + \frac{2R_1}{R_G}\right)(V_1 - V_2) \qquad (1)$$

However, CMRR, especially common-mode gain (*Ac*) of this IA is highly dependent on strict resistor matching [2]. For example, if only 0.1% mismatch between R_5 / R_3 and R_6 / R_4, CMRR deteriorates from ideal (infinity) to 66 dB, on condition that differential gain is 0 dB [5]. Thus, resistor mismatches are serious problem for IA.

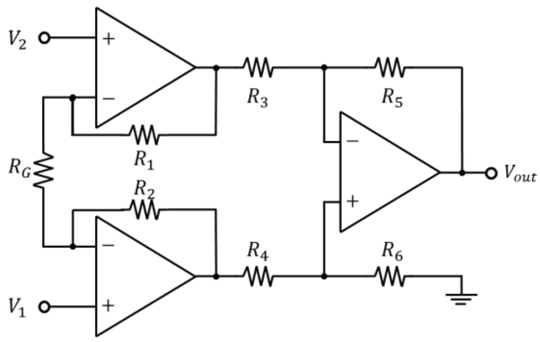

Fig.1. Conventional IA

To overcome this problem, we have proposed an IA architecture which consists of Fully Balanced Differential Difference Amplifier (FBDDA) and Differential Difference Amplifier (DDA) [4]. Its CMRR is extremely higher than that of the conventional IA under the condition of resistor mismatch [3].

On the other hand, in a signal processing system, one of the considerable characteristics is the bandwidth.

Especially, in the biological signal processing, the chopper stabilization technique is often employed for avoiding $1/f$ noise in MOS devices [4]. In this kind of signal processing, wide bandwidth circuits are required strongly. However, the conventional IA exhibits a narrow bandwidth that is highly dependent on the closed-loop gain, due to the fixed gain bandwidth product.

In this paper, high CMRR and wideband IA, which consists of FBDDA and DDA using current feedback technique, is presented. The proposed IA has advantages that common-mode gain is insensitive to the resistor mismatches and bandwidth is wider than the conventional one and is independent of gain. The proposed IA is evaluated through HSPICE with the set of the parameters of 0.6μm CMOS process. In this paper, we report the detailed simulation results.

2. Voltage Feedback and Current Feedback

Voltage feedback is majority feedback method for the conventional IA. Fig.2 shows the block diagram of voltage feedback. $A_{(s)}$ is the open-loop gain as a function of frequency, β is a feedback factor which is amount of feedback from output. Fig.3. represents frequency response of Fig.2. Fig.3 indicates that if we get higher closed-loop gain reducing β, closed-loop bandwidth will be narrow caused by constant Gain Bandwidth Product (GBP). Therefore, IA with voltage feedback is not suitable for implementation of IA with the chopper stabilization technique and high gain.

Fig. 4 shows the block diagram of current feedback. $Z_{(S)}$ is the open-loop trans-impedance gain as a function of frequency, g_{in} is a trans-conductance which converts input voltage to current, g_f is a trans-conductance which feedback output signal as current. Fig.5 denotes typical frequency response of Fig.4. As long as g_f is fixed, the bandwidth is constant, even if the closed-loop gain is varied by changing g_{in} [6]. Therefore, current feedback has wider bandwidth than voltage feedback, and its bandwidth is independent of the closed-loop gain. Therefore, the current feedback is suitable for high gain IA with the chopper stabilization technique.

3. Proposed Instrumentation Amplifier

Fig. 6 shows the proposed architecture for the high CMRR and wideband IA. The proposed IA consists of 1st stage and 2nd stage shown in Fig.6. 1st and 2nd stages are designed based on FBDDA and DDA respectively, and FBDDA and DDA are realized by using 2nd generation Current Conveyors (CCII) and buffers for implementation of current feedback. As for CCII,

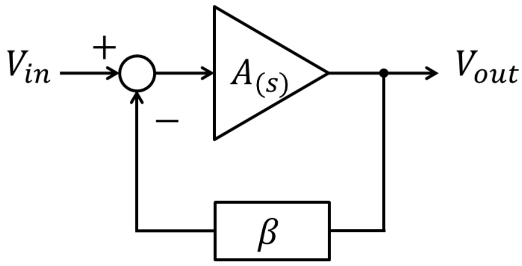

Fig.2. Block Diagram of Voltage Feedback

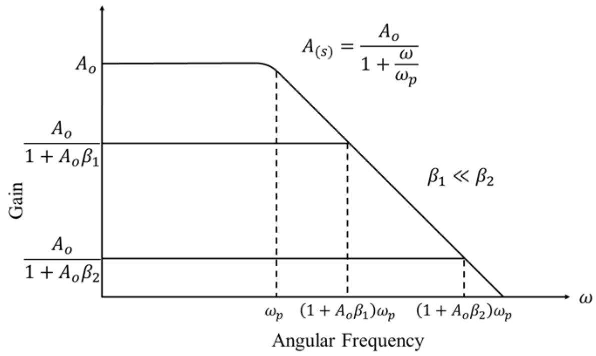

Fig.3. Frequency Response of Voltage Feedback

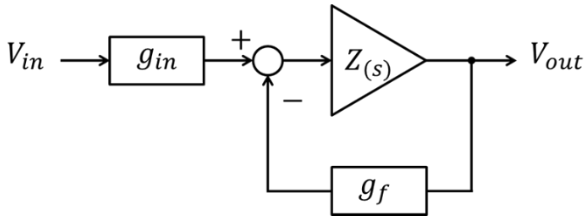

Fig.4. Block Diagram of Current Feedback

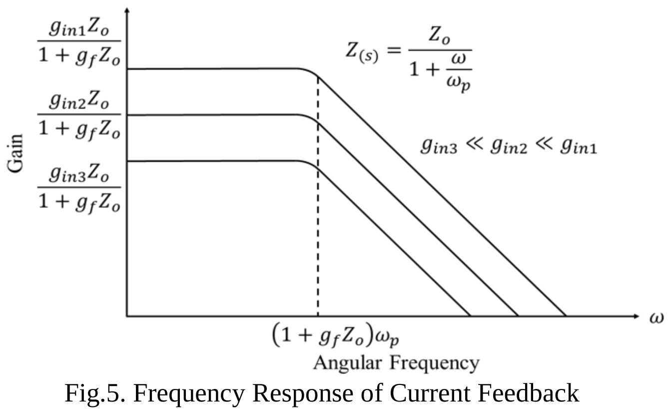

Fig.5. Frequency Response of Current Feedback

terminal Y_i (i=1, 2, 3) exhibits an infinite input impedance in ideal, the voltage at X_i (i=1, 2, 3) follows that applied to Y_i, X exhibits a zero input impedance in ideal. The current supplied to X is conveyed to the high impedance output terminal Z_i [7]. Theoretically, each resistors of the proposed IA no require resistor matches for high CMRR. Furthermore, the proposed IA has higher closed-loop gain over a larger bandwidth than corresponding conventional IA.

The output voltage of 1st stage (V_A and V_B) is given as follows in the case of $R_1 = R_2$.

$$V_A = \frac{1}{2}\left(1+\frac{2R_1}{R_G}\right)(V_1 - V_2) \qquad (2)$$

$$V_B = -\frac{1}{2}\left(1+\frac{2R_1}{R_G}\right)(V_1 - V_2) \qquad (3)$$

From Eq. (2) and (3), common-mode signal can be rejected at V_A and V_B before 2nd stage. In addition, output voltage of 2nd stage is given by

$$V_{out} = \left(1+\frac{R_4}{R_3}\right)(V_A - V_B) \qquad (4)$$

Then, from Eq. (2), (3) and (4), we can derive V_{out} as follows.

$$V_{out} = \left(1+\frac{R_4}{R_3}\right)\left(1+\frac{2R_1}{R_G}\right)(V_1 - V_2) \qquad (5)$$

In mismatch condition ($R_1 \neq R_2$), $V_{out,m}$ can be given by

$$V_{out,m} = \left(1+\frac{R_4}{R_3}\right)\left(1+\frac{R_1+R_2}{R_G}\right)(V_1 - V_2) \qquad (6)$$

Eq. (6) represents common mode signal is rejected even if the mismatches in all resistors are occurred. Thus, the proposed IA has much higher CMRR than the conventional one.

4. Simulation Results

In this chapter, simulation results of CMRR and frequency response are shown. The conventional IA and proposed IA were evaluated using HSPICE with 1P 3M 0.6μm CMOS process.

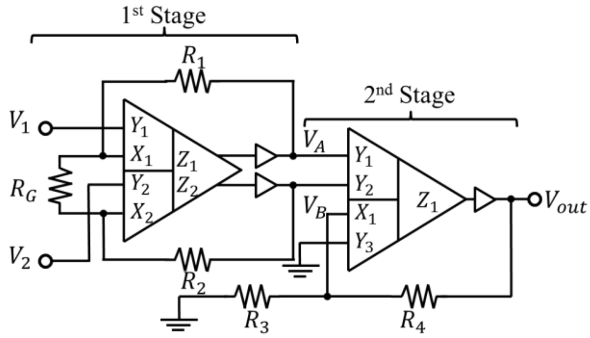

Fig.6. Proposed IA

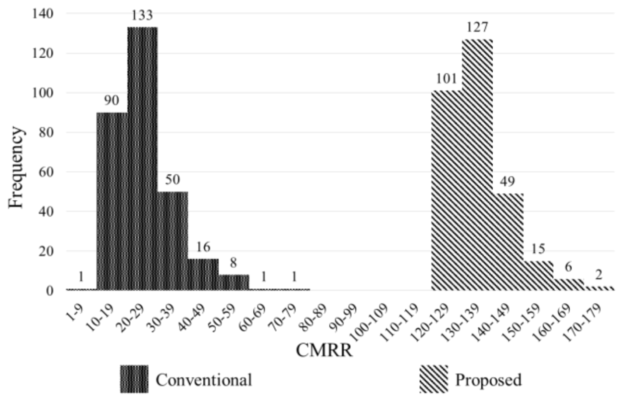

Fig.7. Histogram of CMRR

4.1. *CMRR*

For comparison of conventional and proposed IA, we have simulated 300 times with ±30% all resistor mismatches by Monte Carlo analysis. The simulation result is shown in Fig.7. To evaluate the effect of A_C which is more sensitive to resitor mismatch than differential gain (A_D), A_D of both IAs are set 0 dB for easy estimation.

From Fig. 7, average CMRR of conventional and proposed IA are 24.9 dB and 134.2 dB respectively. The average CMRR of the proposed IA is 109.3 dB higher than conventional one.

4.2. *Frequency Response*

Fig.8 and Fig.9 show the frequency response of the conventional IA and proposed IA, respectively under the condition that the differential gain of both IAs are varied from 12 dB to 20 dB by changing R_G. As closed-loop gain of the conventional IA is getting higher, the cut-off frequency is getting lower. On the other hand, the cut-off frequency of the proposed IA is constant, regardless of change of the closed-loop gain. Therefore, proposed IA is superior to conventional IA in terms of bandwidth.

Lastly, the detailed simulation results are listed in Table 1. From these results, the performance of the proposed IA is much better than that of conventional one.

5. Conclusion

In this paper, high CMRR and wideband current feedback instrumentation amplifier using CCII have been presented. The CMRR and frequency response of conventional and proposed IA were evaluated by HSPICE. As a result, we confirmed the proposed IA has 109.3 dB higher CMRR than the conventional one under the resistor mismatches. Moreover, it was verified proposed IA has higher closed-loop gain over a larger bandwidth than corresponding conventional IA.

The evaluation through the actual fabrication of the LSI is the future work.

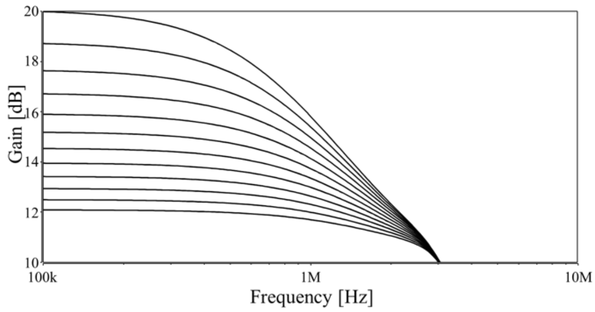

Fig.8. Frequency Response of Convention IA

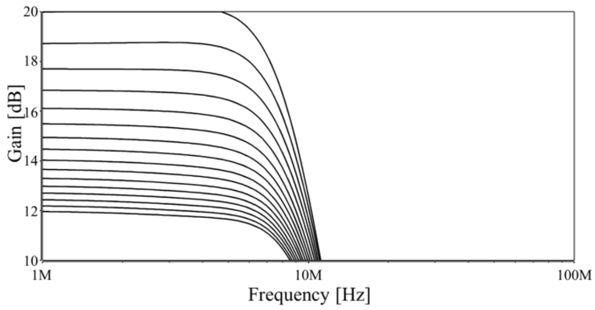

Fig.9. Frequency Response of Proposed IA

Table 1. Summary of the Simulation Results.

Item	Conventional IA	Proposed IA
	AC analysis	
Cut-off Frequency (Differential Gain = 20 dB)	750 kHz	7.8 MHz
Unity Gain Frequency	5 MHz	16.5 MHz
Power Consumption	2.6 mW	1.6 mW
	Monte Carlo analysis	
Average CMRR (Differential Gain = 0dB)	24.9 dB	134.2 dB

Acknowledgements

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